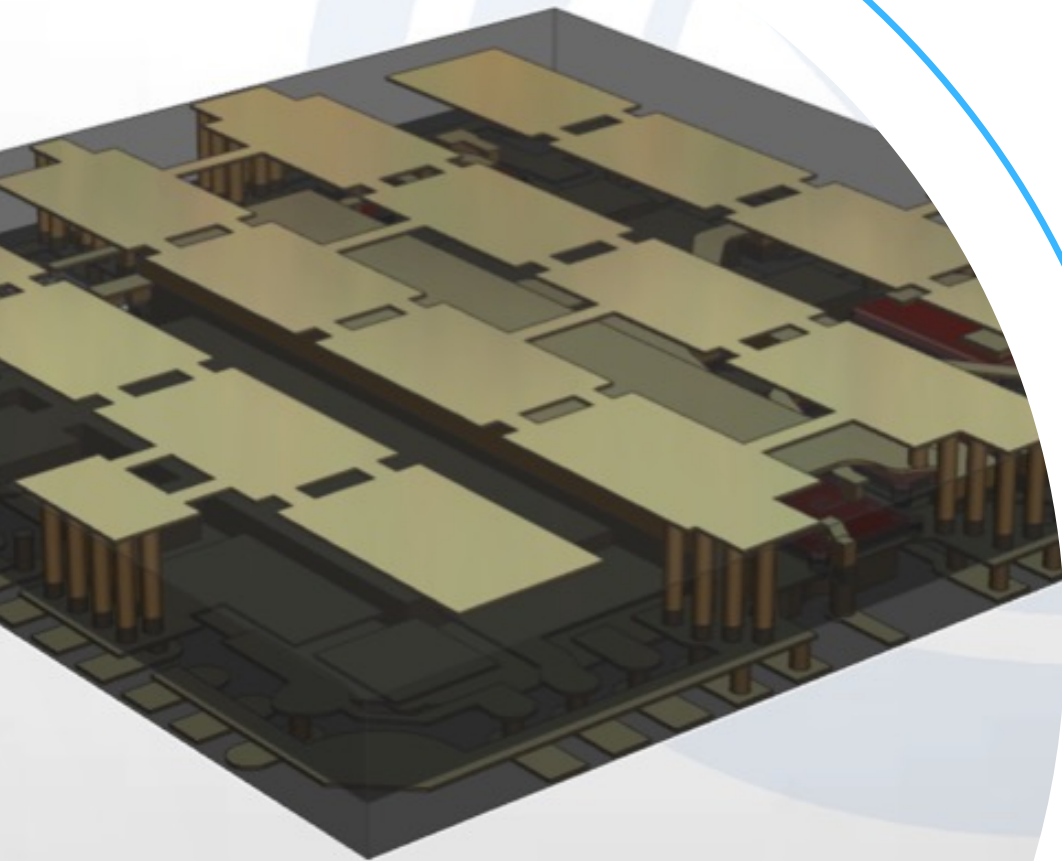


Innovative packaging by AME technology

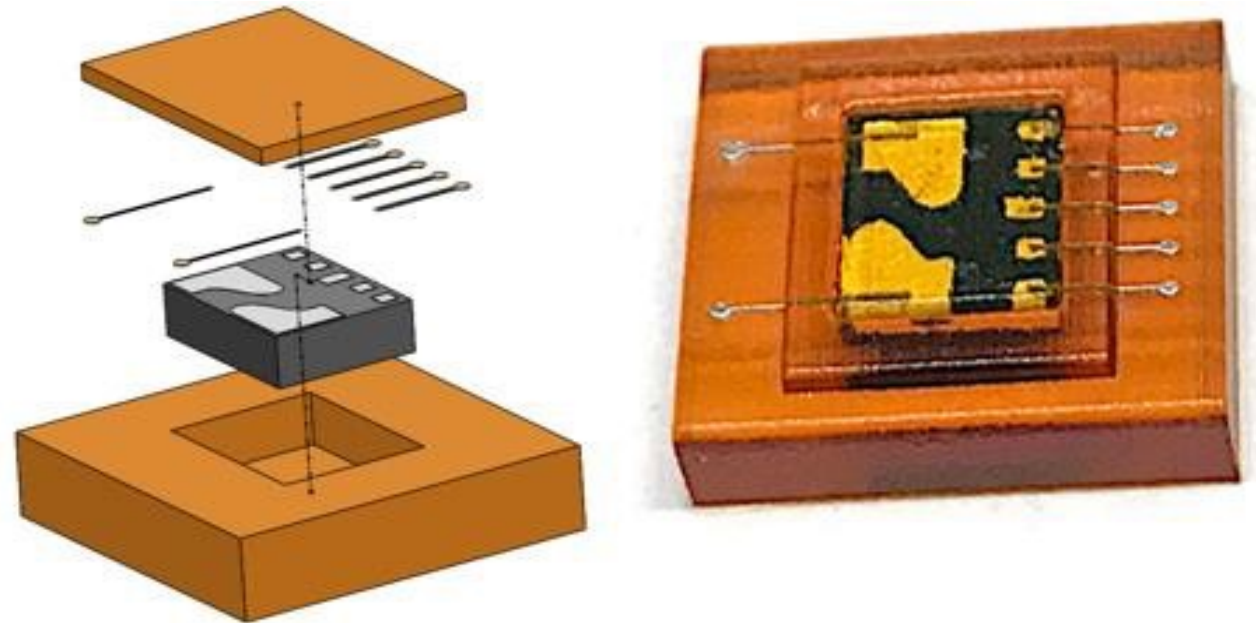
DR. RAFAEL DEL REY

August 2023

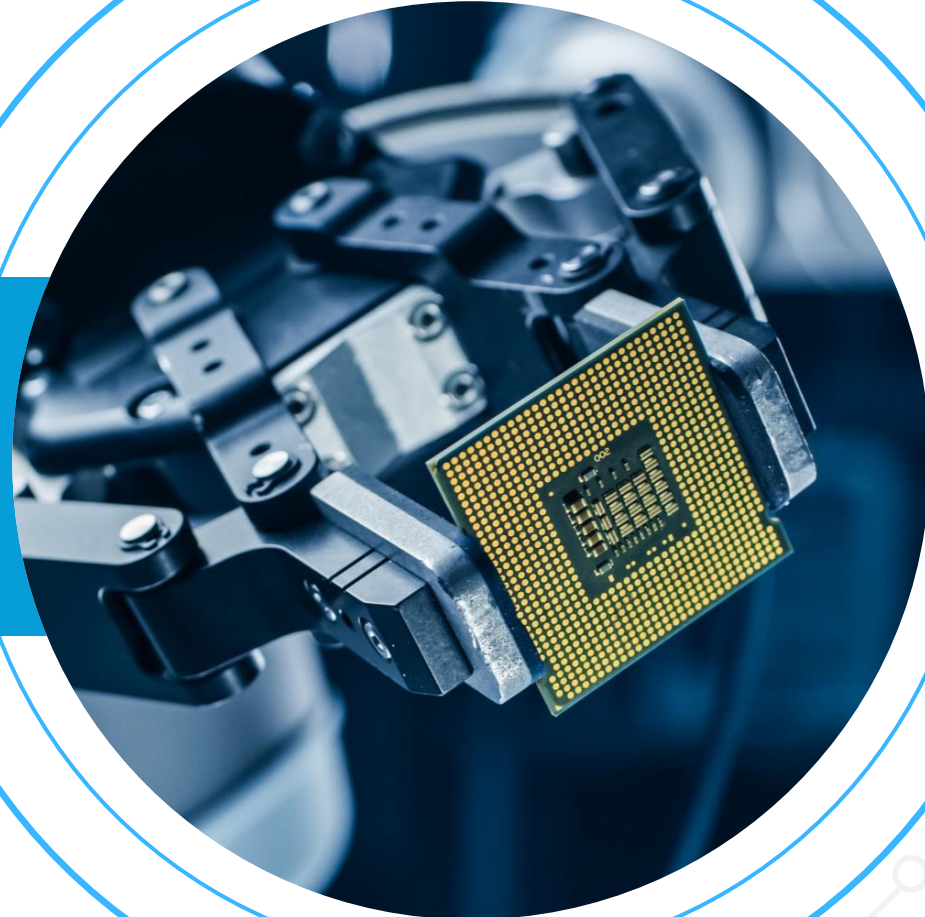


Agenda

- Introduction
- Motivation
- AME Packaging History & Process Evolution
- AME Description
- System in Package (SiP) Development Flow
- RF SiP
- Power Transistor AME Packaging
- Summary



AME Packaging

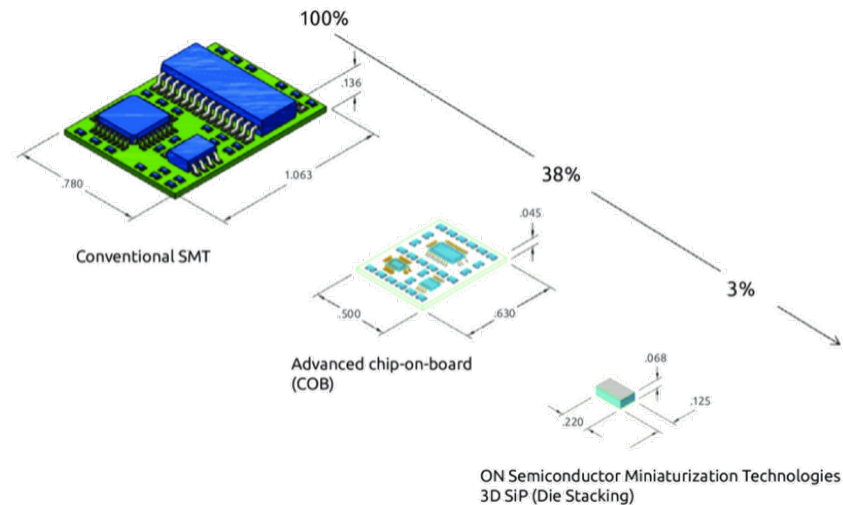


Motivation

CURRENT WORLD OF ELECTRONICS

1. Limits:

preventing improvement of performance and reduction other factors such as weight and size



Weight and size over 90% down

2. Supply chains:

hurting most in the high variety small mix and when prototyping (long R&D cycles)



Motivation (cont.)

TRADITIONAL MANUFACTURING VS. SUSTAINABLE AM SOLUTIONS

3. Sustainability

A holistic approach towards functional electronics with net zero carbon emissions



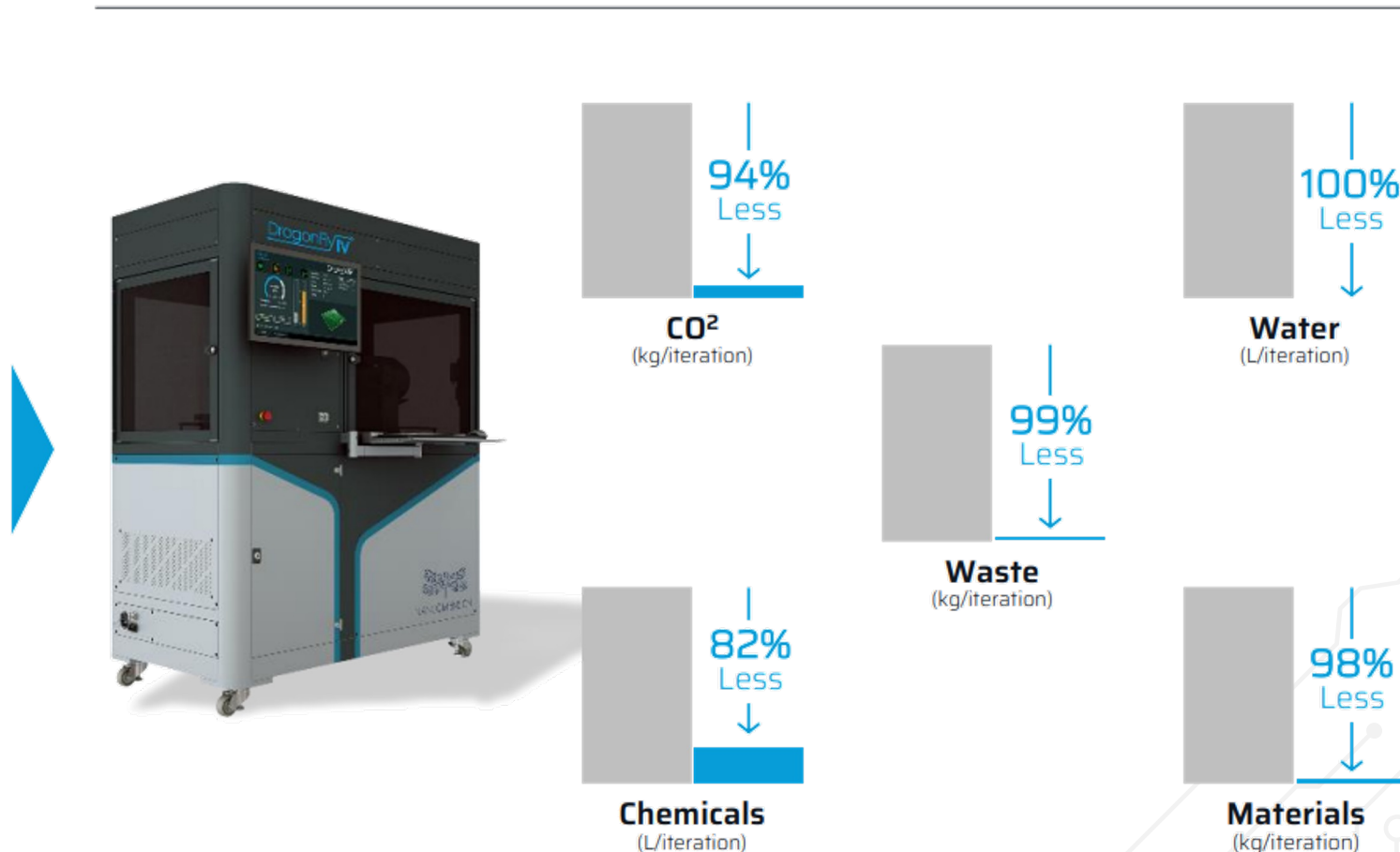
Motivation (cont.)

TRADITIONAL MANUFACTURING VS. SUSTAINABLE AM SOLUTIONS

Before



After



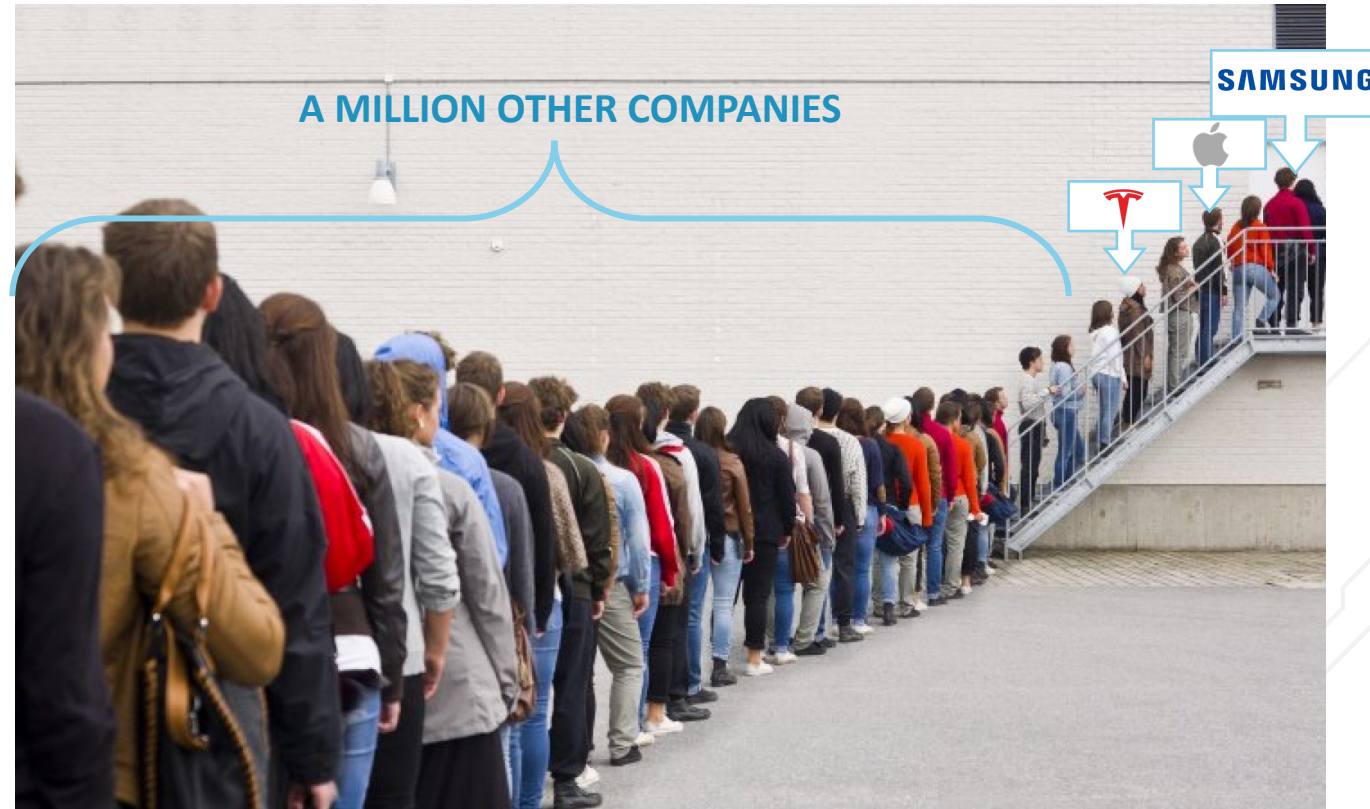
¹ Based on a 2021 study by HSSMI, a UK based sustainability consultant

Motivation (cont.)

LONG LINES FOR PACKAGING AND PROTOTYPING

Very long lead time for small & medium-sized enterprises and very long R&D-cycles

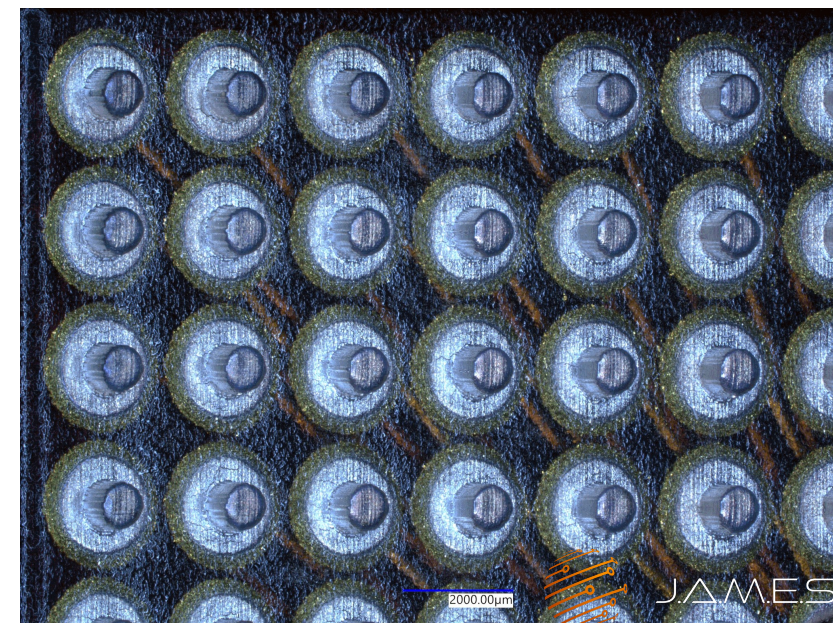
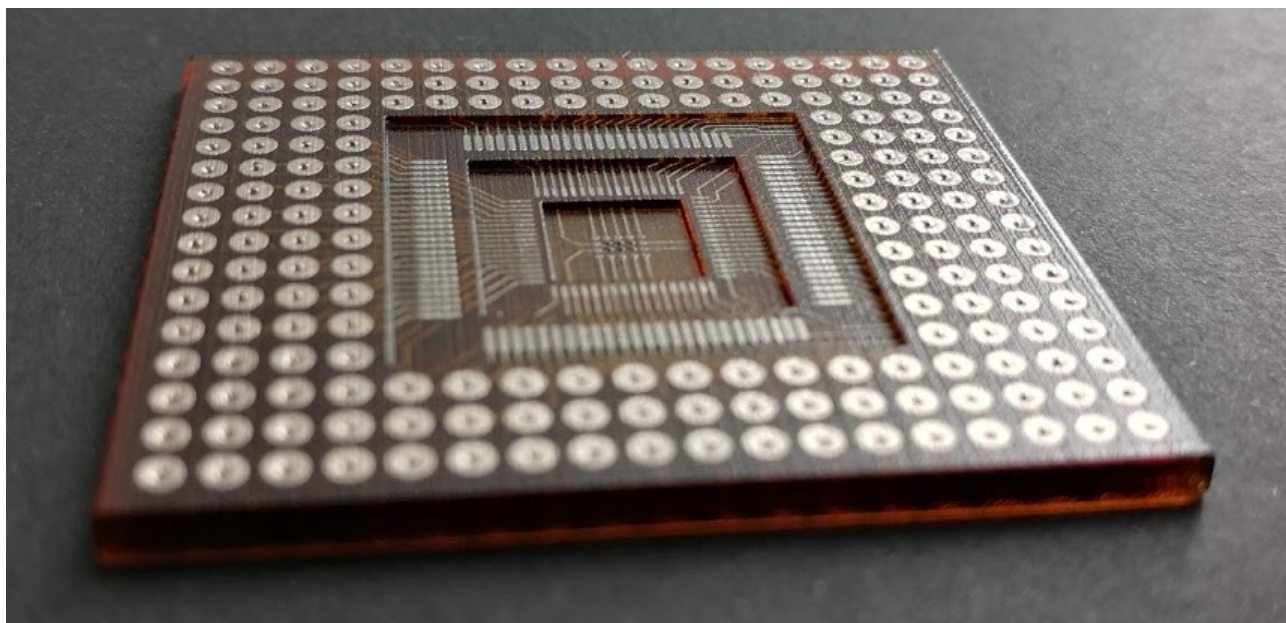
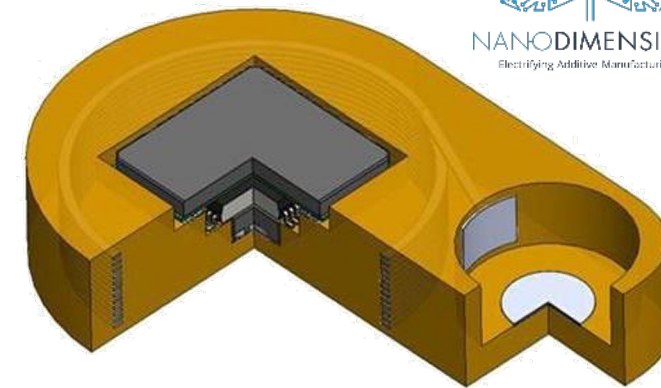
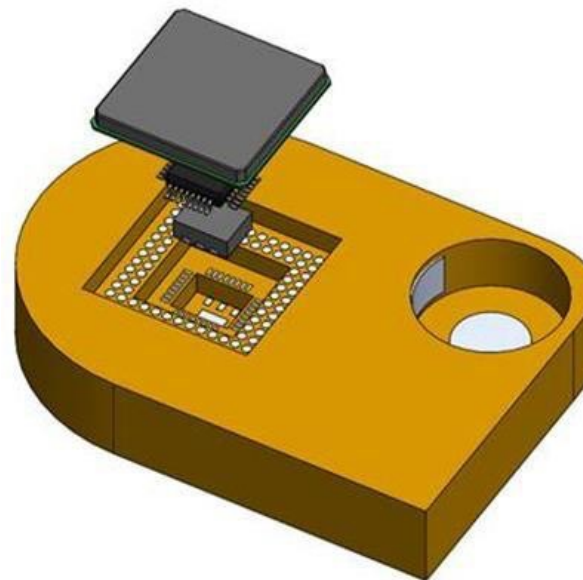
- To produce a prototype, 4 R&D cycles are required
- each cycle has a 3-4 months lead time until supplied from the global packages & electronics manufacturer



History

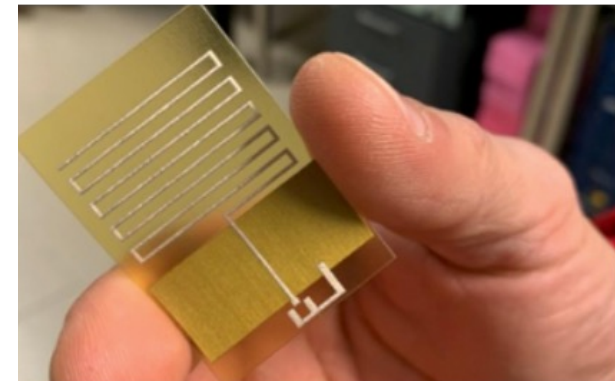
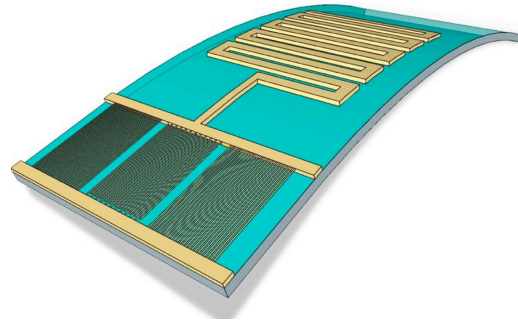
AME SOCKETS & INTERPOSERS

- Very first encapsulation concept: Stacking of packaged ICs and interposers



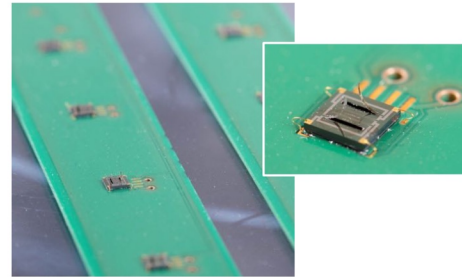
History (cont.)

AME SENSOR APPLICATIONS

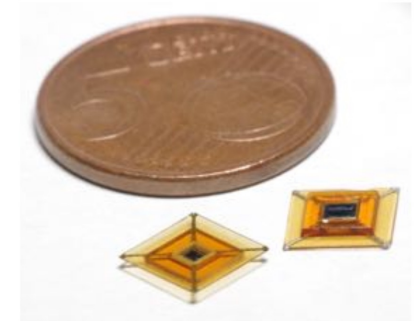


Compact and flexible meander antenna for Surface Acoustic Wave sensors

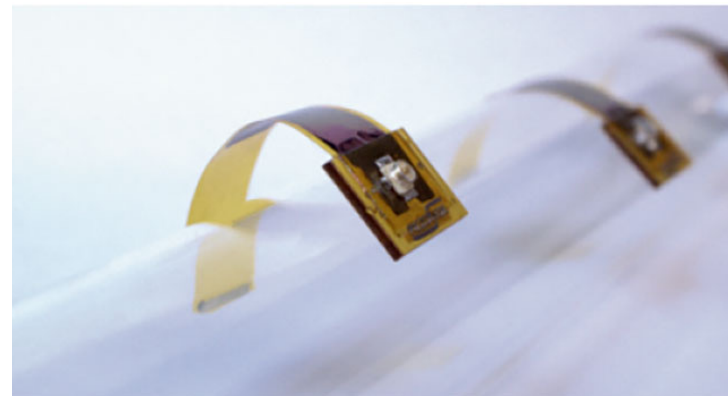
Artificial Hair Cells for Flow Sensing



EMBEDDING FLOW SENSORS IN SEALED PACKAGE



Sensor direct print packaging (3D printed wirebonding)



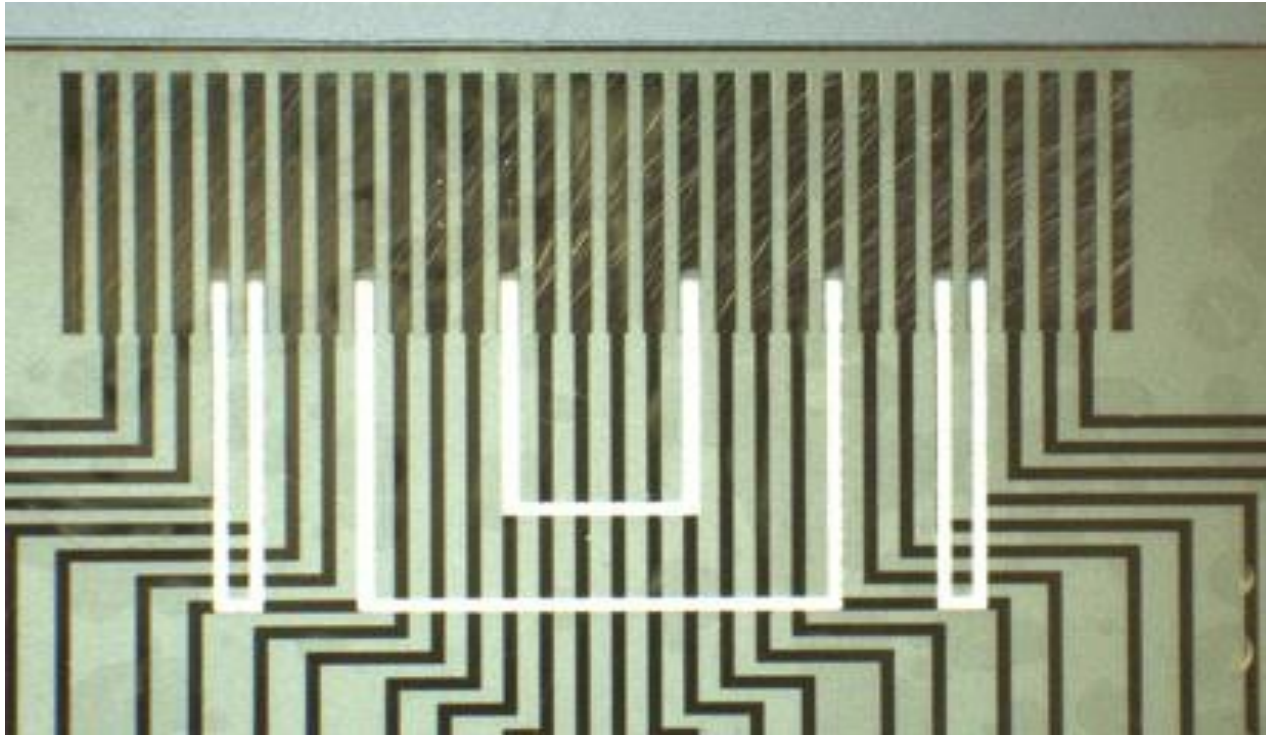
3D embedded sensor in electrical packaging



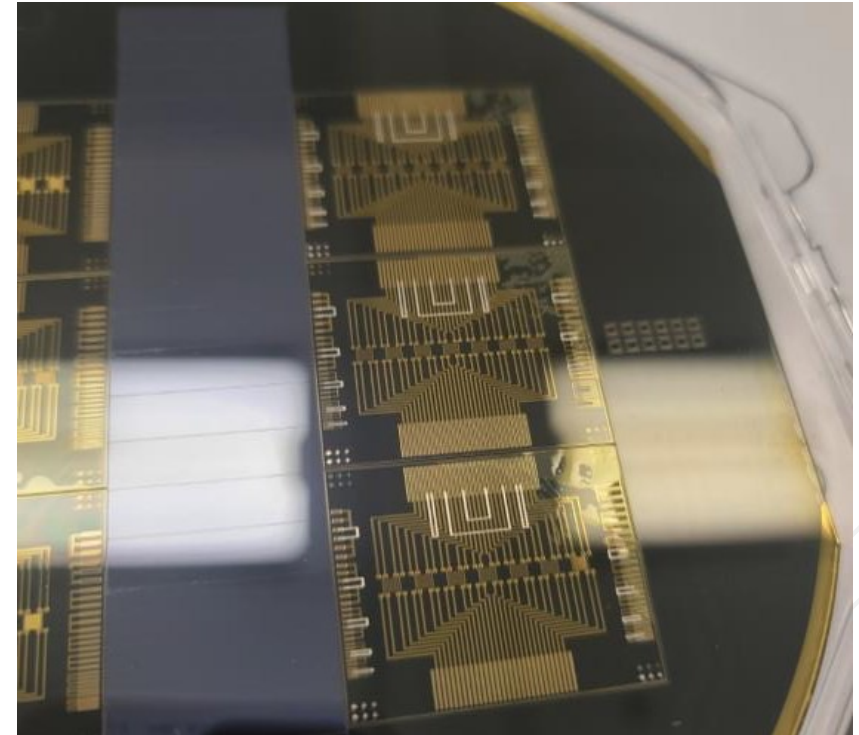
Optoelectronic Neural Surface

History (cont.)

TESTPATCH AGCITE® BONDING



Print on foil

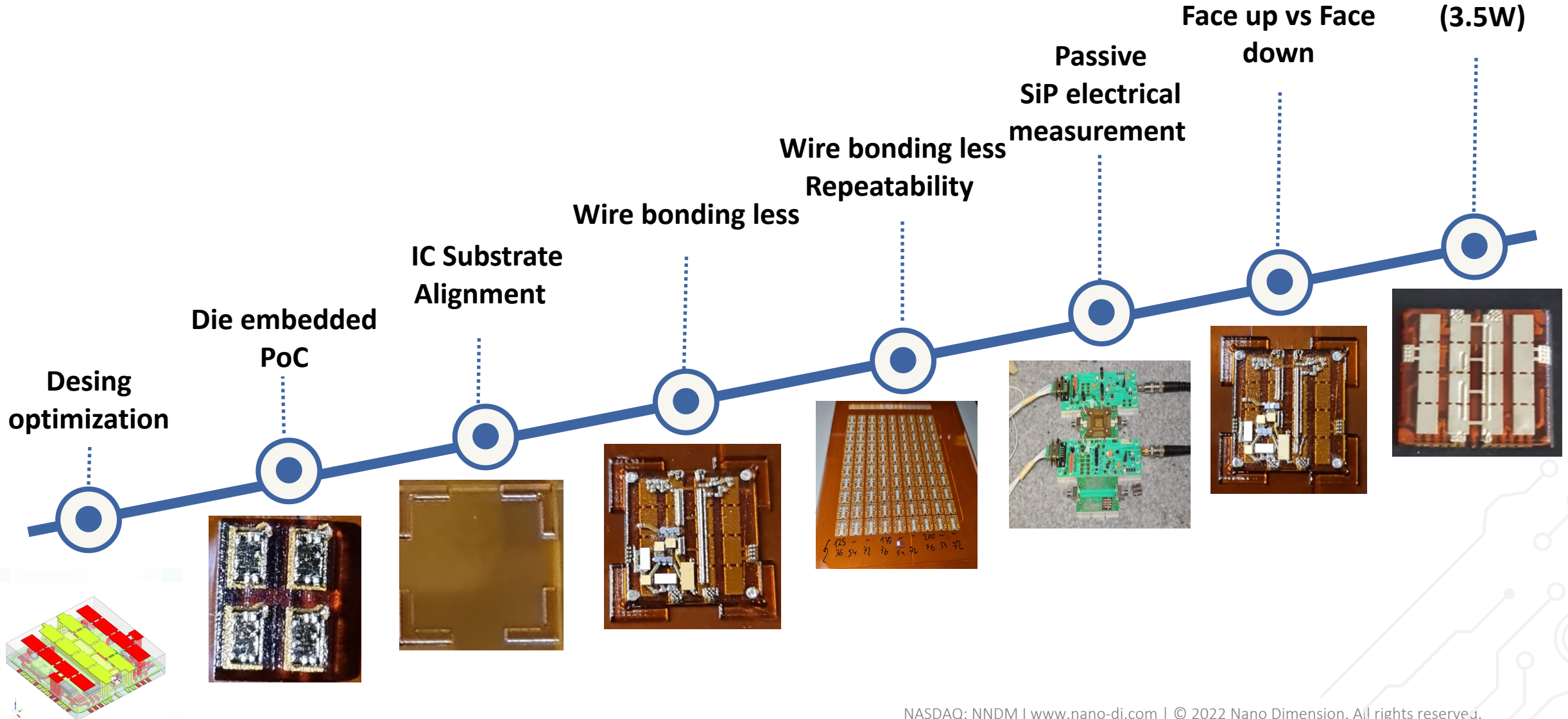


Print on wafer

Process Evolution

PROCESS PLANNING, SYSTEM DESIGN AND DIE IMPLEMENTATION

Functional SiP
(3.5W)

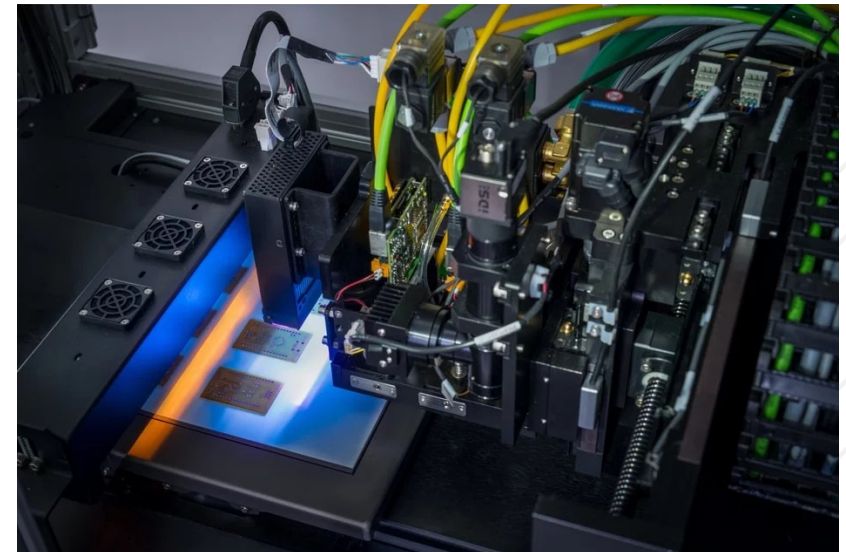
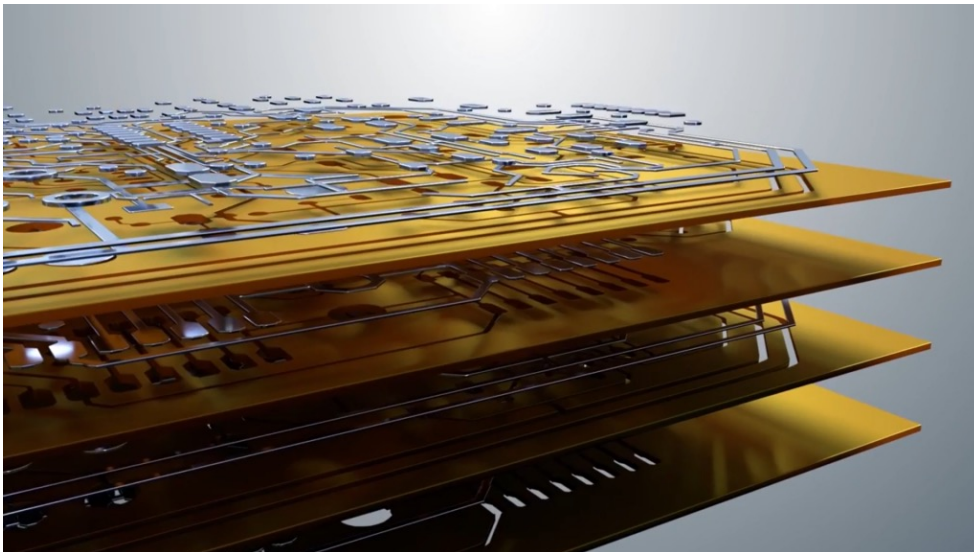


But how it works?

ADDITIVE MANUFACTURING ELECTRONICS (AME) - PROCESS DESCRIPTION

- Inkjet technology that combines UV-cured dielectric material (acrylic monomers) with silver nanoparticles (Ag NP) that undergo sintering upon IR radiation.

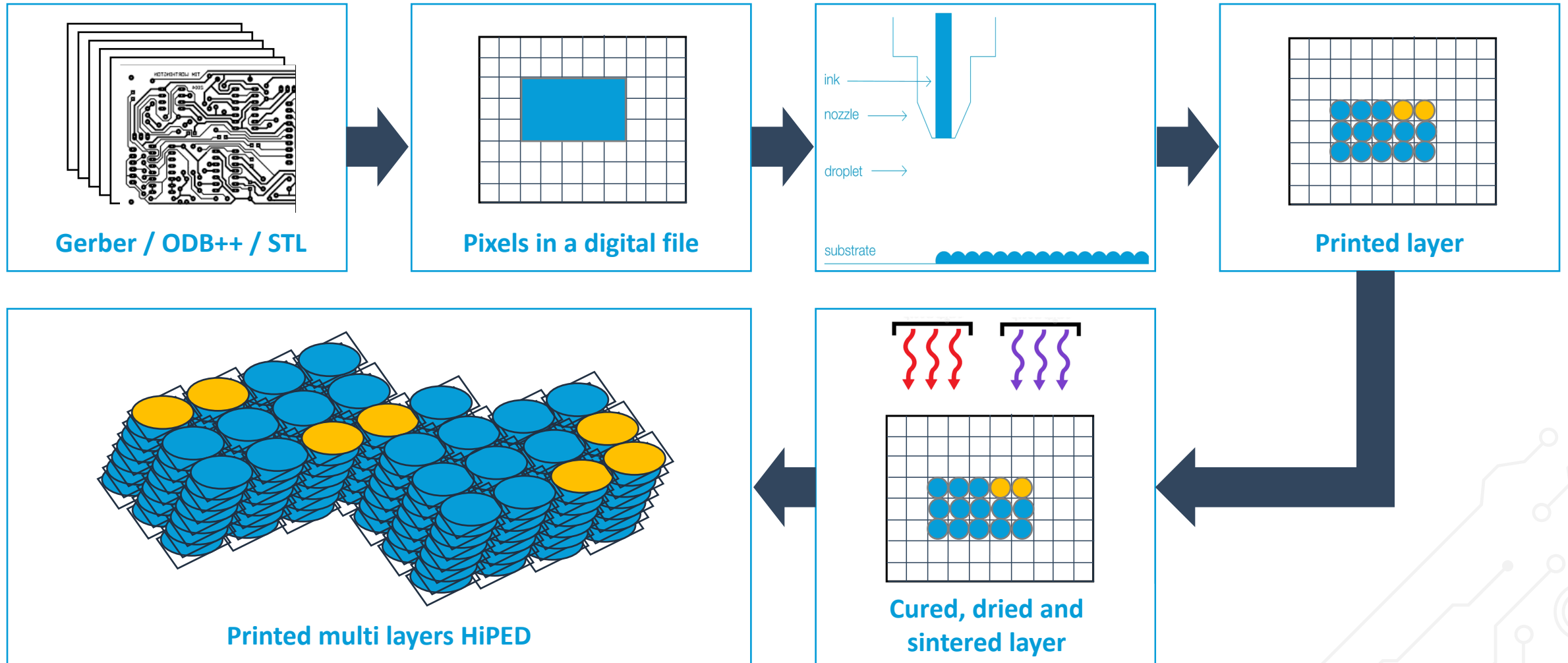
Result in solid objects with highly conductive patterns in shapes unachievable through traditional processes



Additive Manufacturing Electronics (AME) - DragonFly

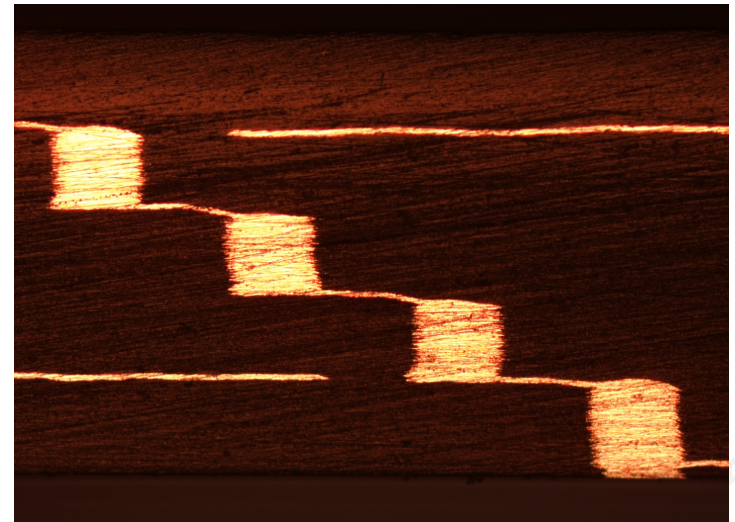
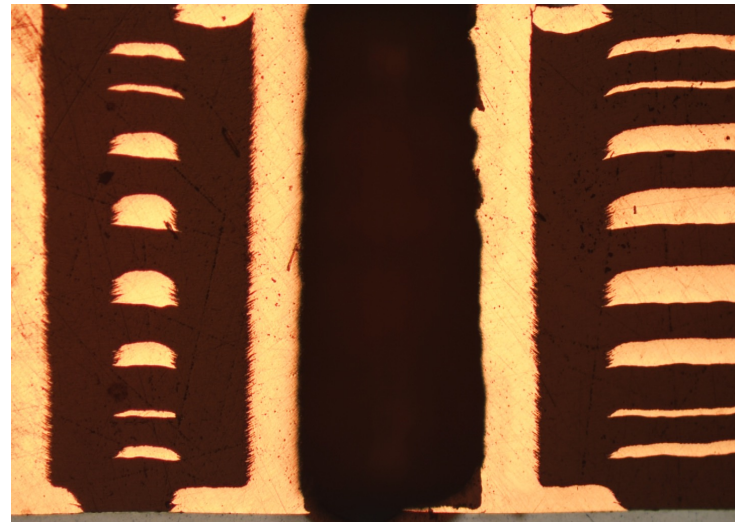
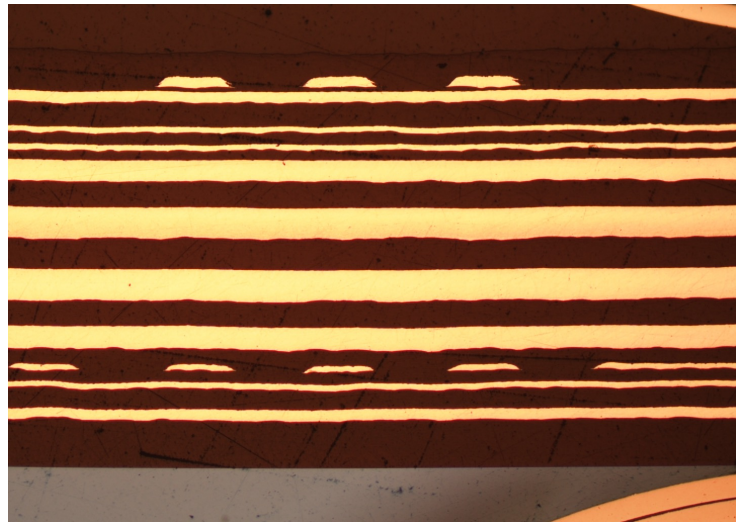


From a Digital design file to a Printed Hi-PED



AME Build

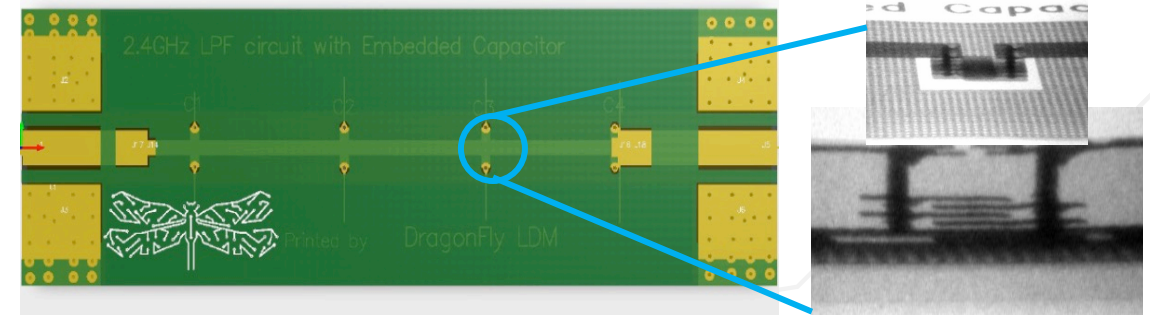
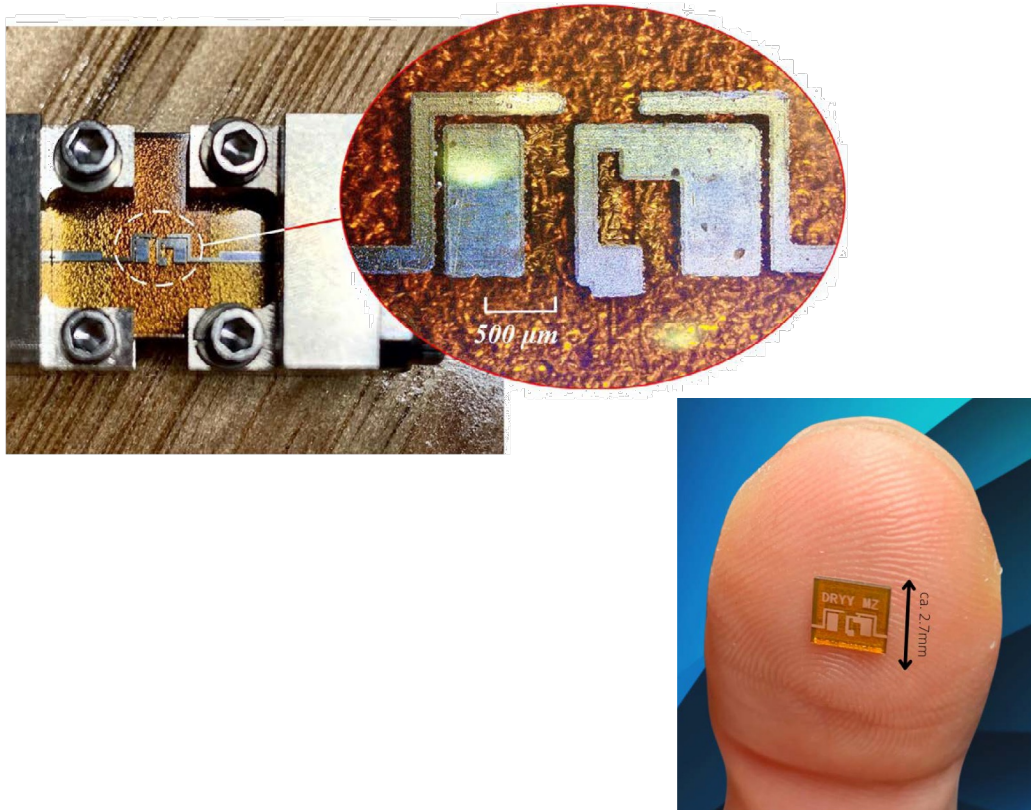
CROSS-SECTIONAL VIEW



RF Examples

HIGH FREQUENCY FILTERS

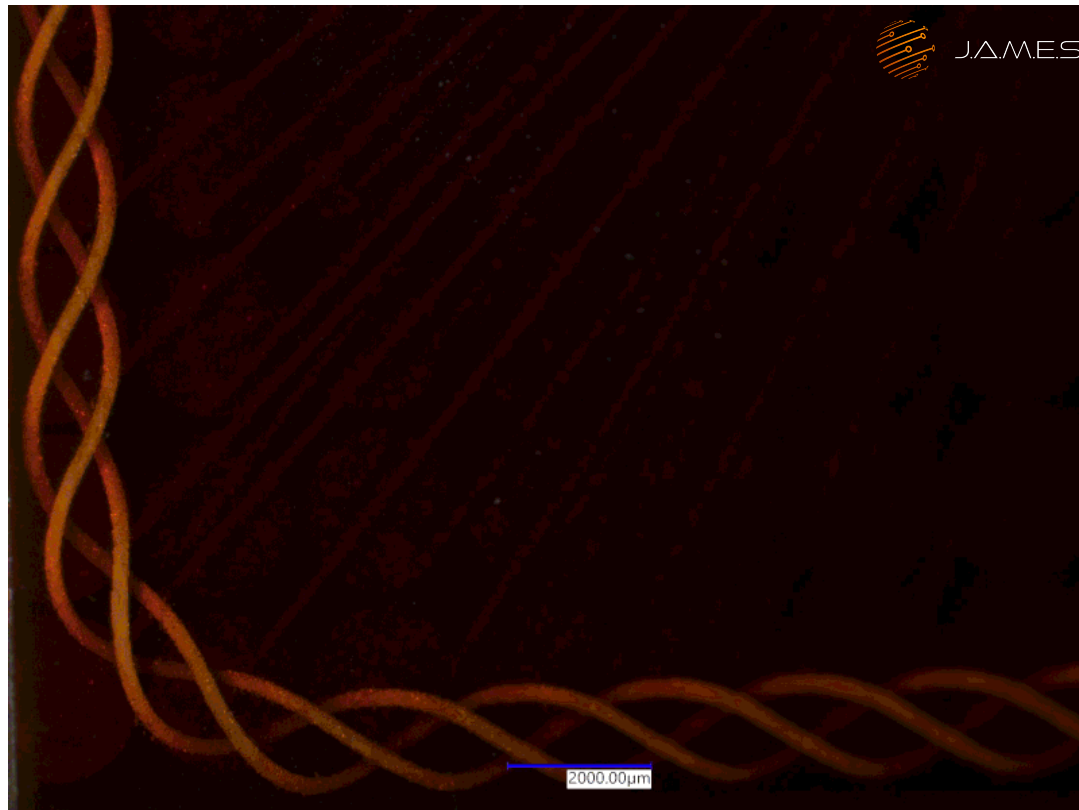
- Complex tuning iterations and extra laser trimming process is replaced by an overnight print



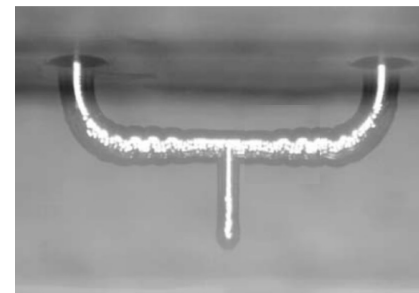
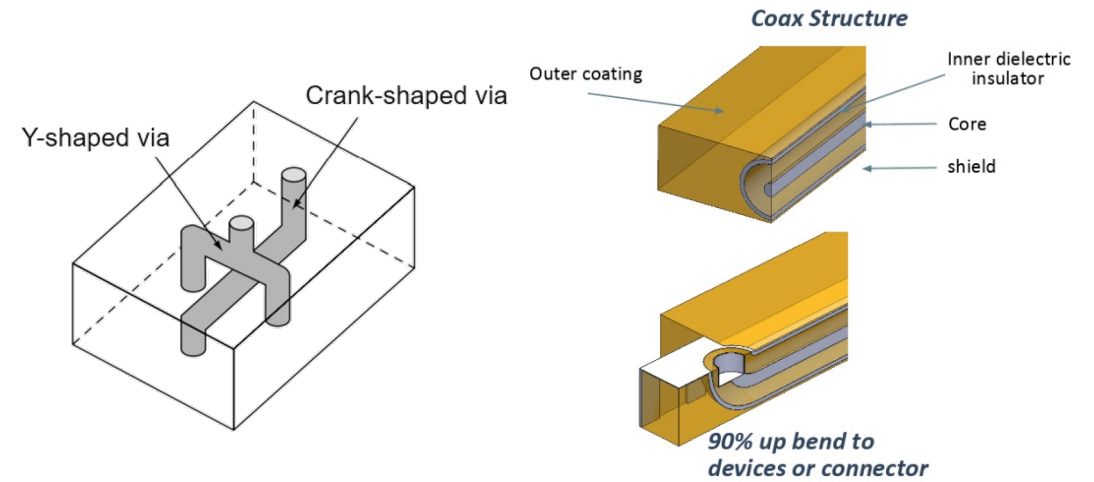
New Design Thinking

NON PLANAR TRANSMISSION LINES

- Coaxials, twisted pairs, waveguides. Freedom of via interconnects



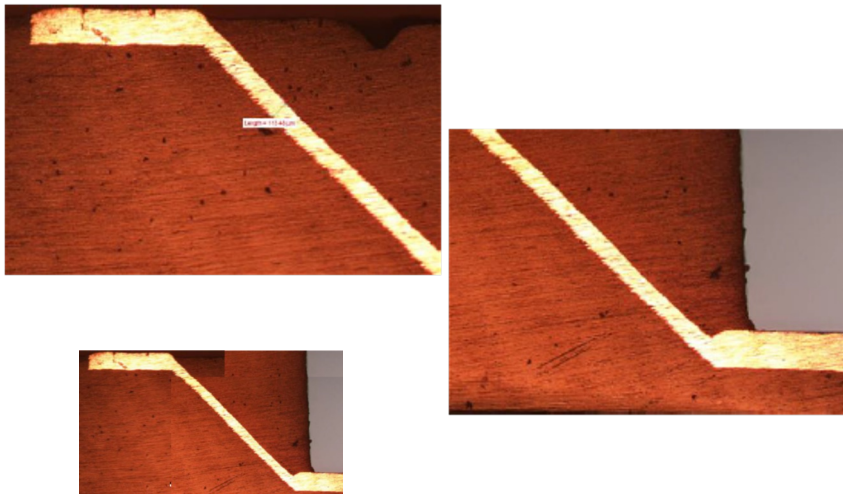
Source: J.A.M.E.S



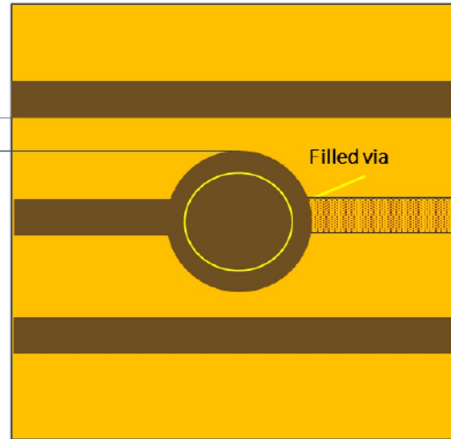
New Design Thinking

HIGHER DENSITY ROUTING

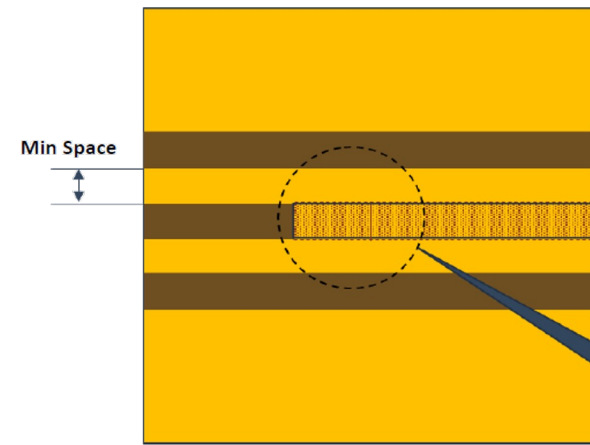
- Homogeneous Z-axis structures allow to 45 degrees vias with increased performance and space reduction



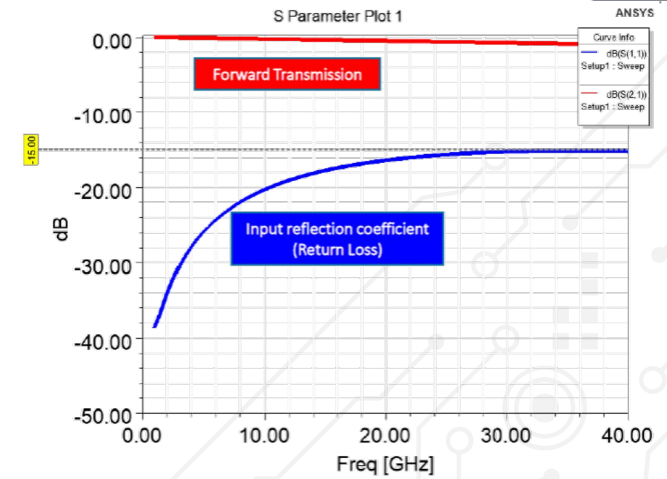
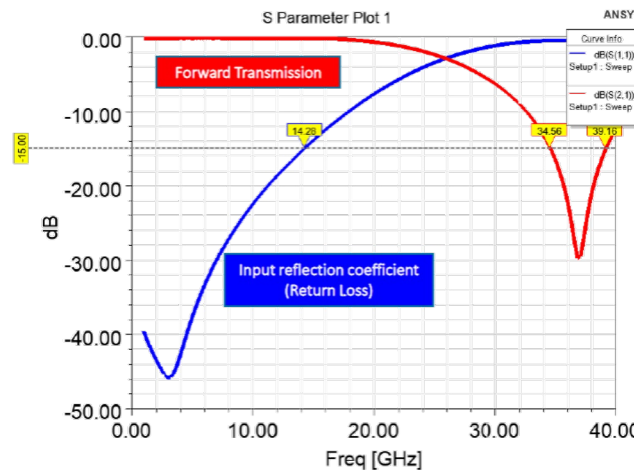
Traditional PCB Process



3D AME Process



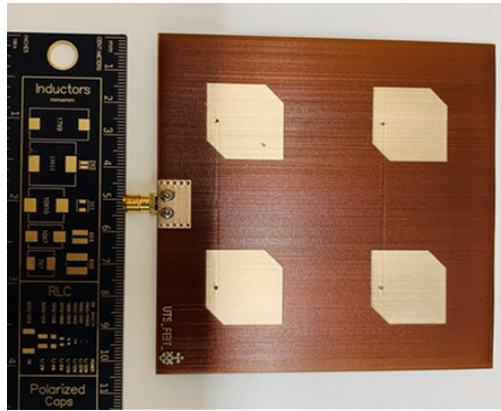
Traditional VIA and pad location



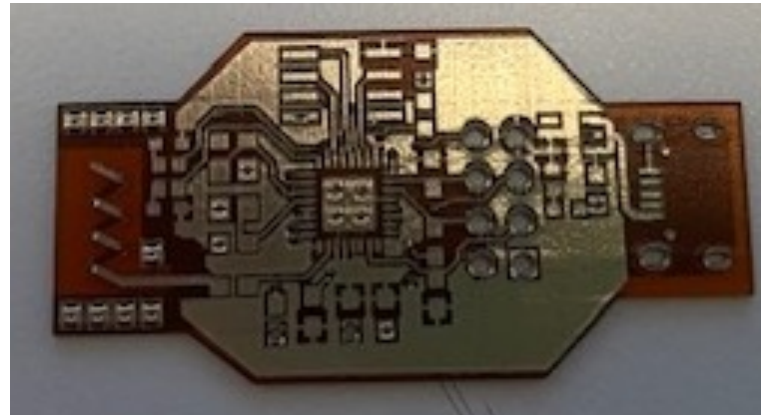
New Design Thinking

3D-PRINTED ANTENNAS AND RESONATORS

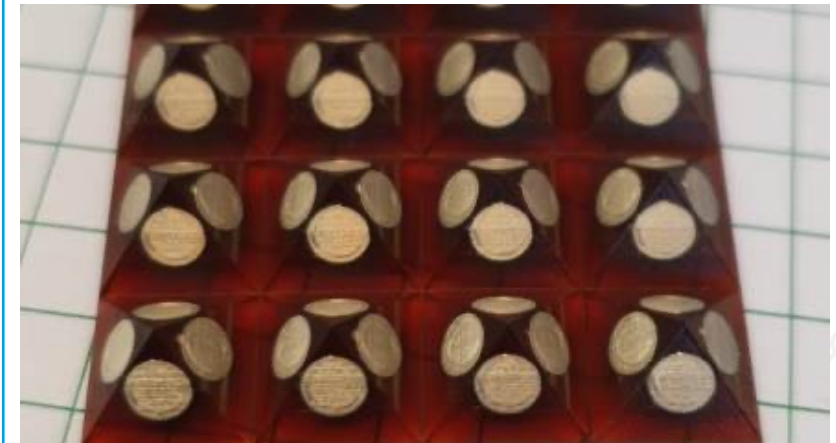
- AME technology is an enabler for new designs of antennas
- Design freedom in the 3D space enables unique antennas such as:
Omni directional antennas, coils antennas, special shaped phased-array antennas, etc.



Patch Antenna



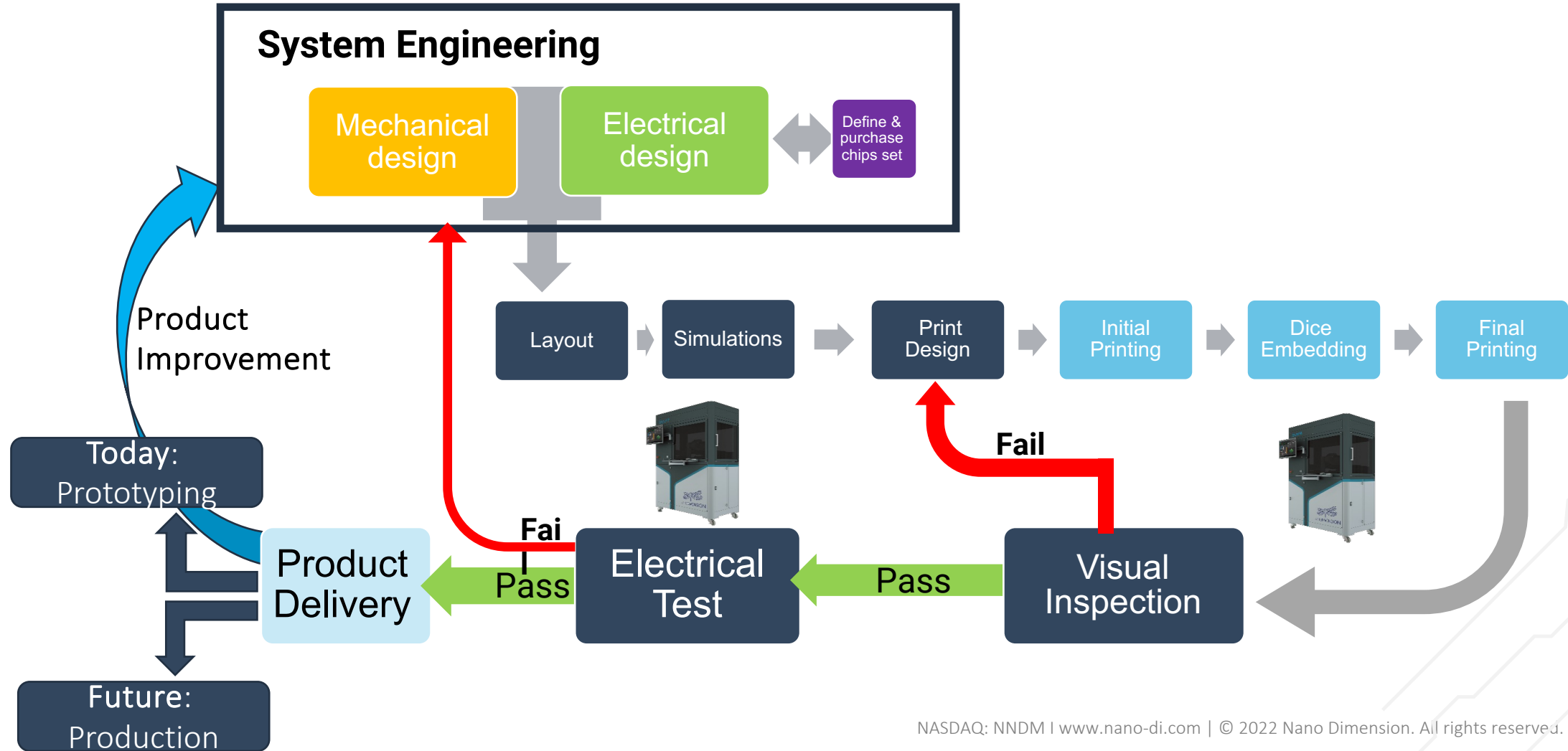
Metamaterial Antenna



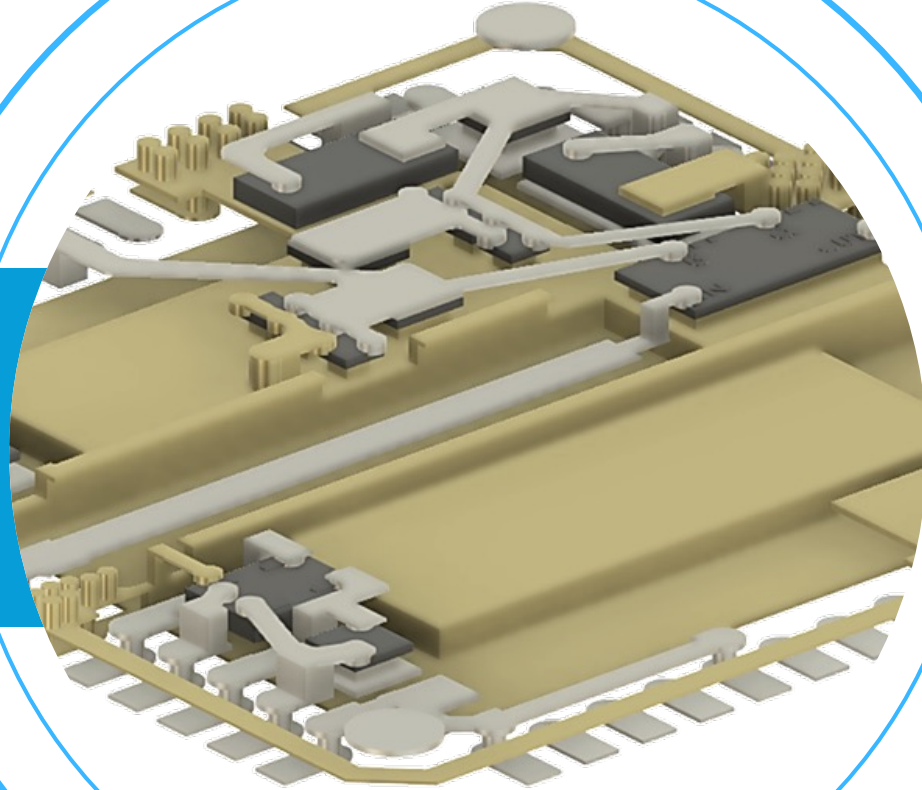
Sphere phase array Antenna

System in Package (SiP) development flow

PROCESS PLANNING, SYSTEM DESIGN AND DIE IMPLEMENTATION

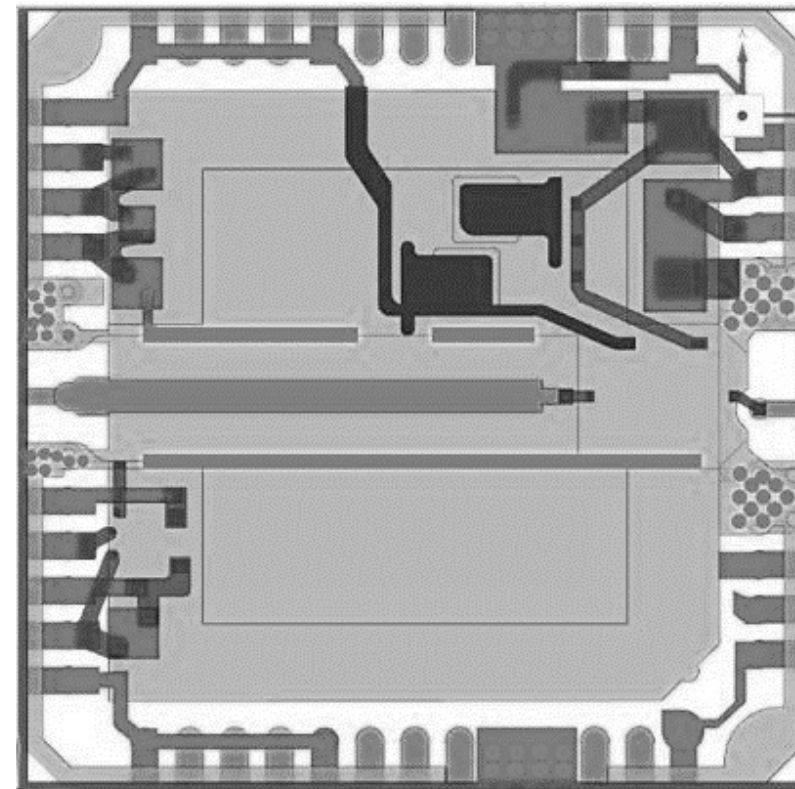
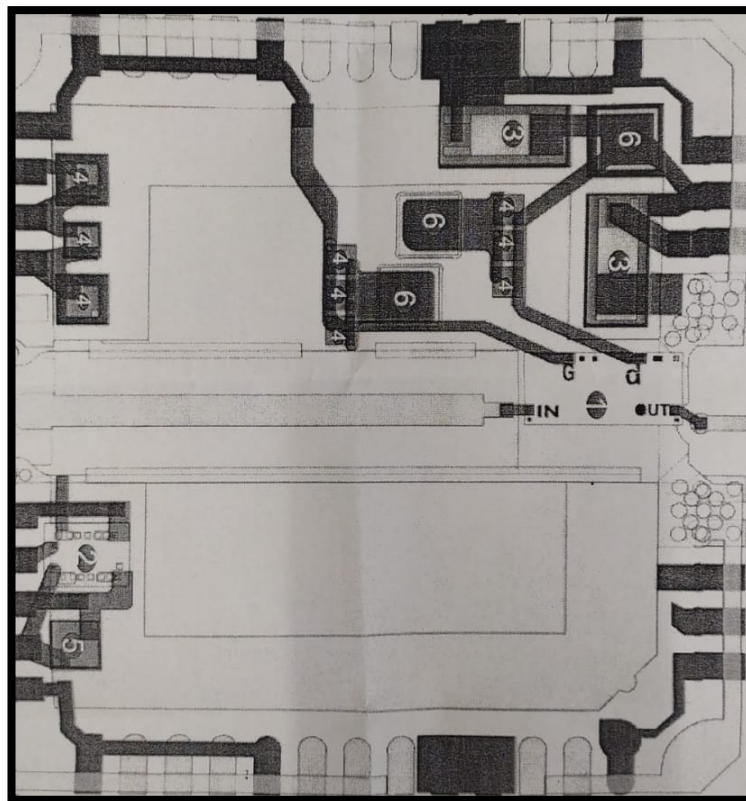


RF SiP



Schematic

- Main component:
 - MMIC 4W X-band die (QPA1022D)
- Other: Resistors (6), capacitors (3) and MOSFET dies.



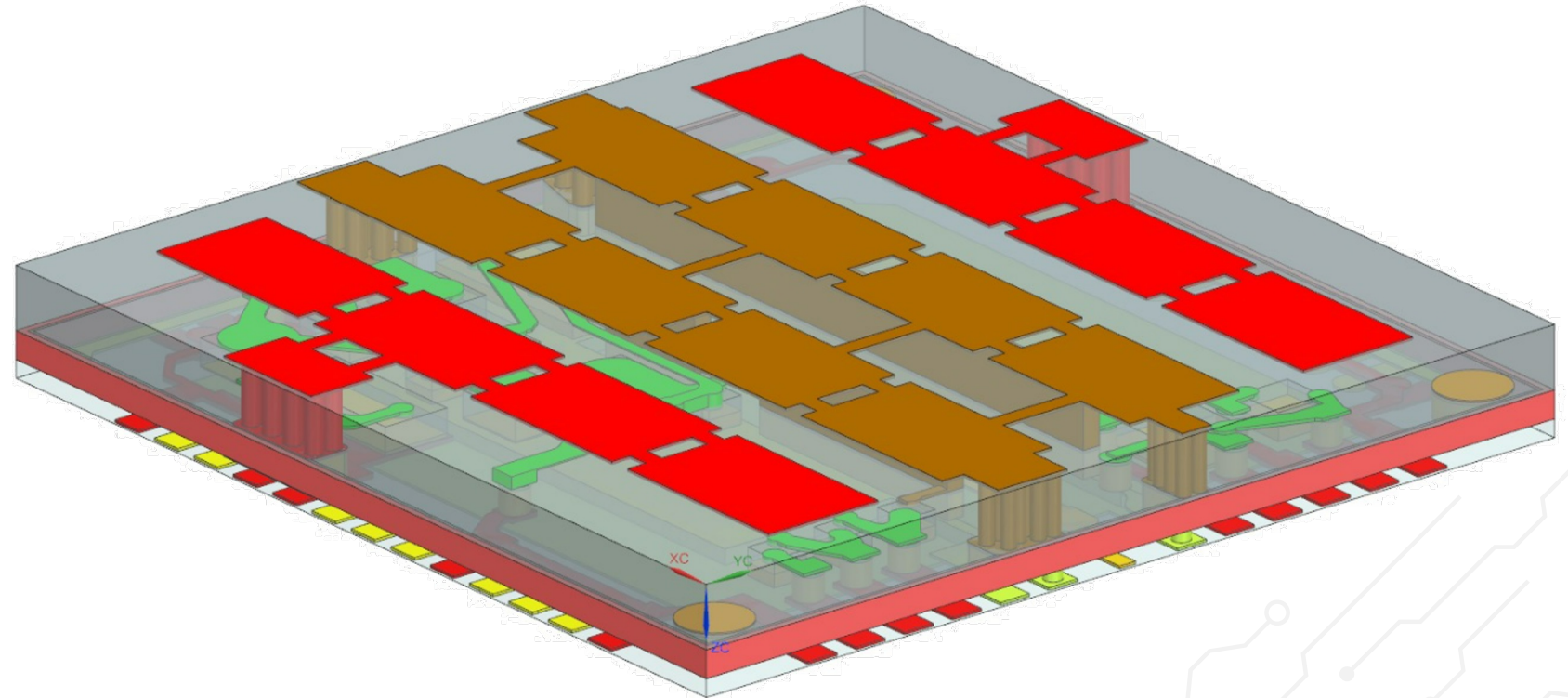
Layout and BOM

- Main component:
 - MMIC 4W X-band die (QPA1022D)
- Other: Resistors (6), capacitors (3) and MOSFET dies.
- Overall physical dimensions:
 - 13.2x13.2x1.5mm
- Minimum pad size on die 80um.

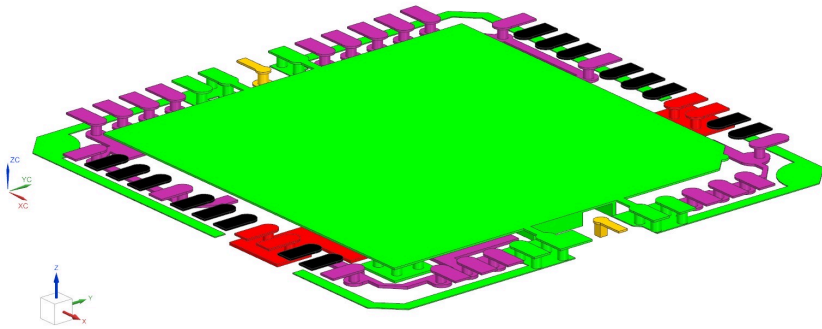
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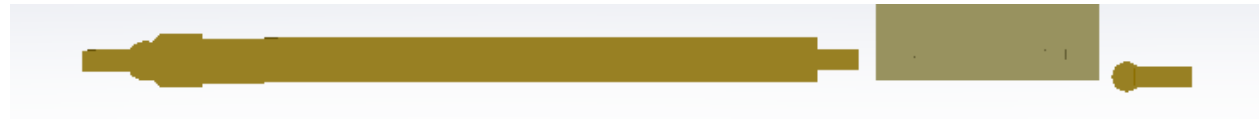
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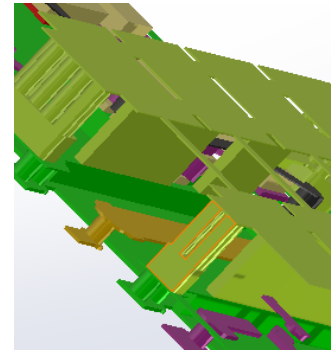
Layout and BOM –cont'



- QFN on bottom side.

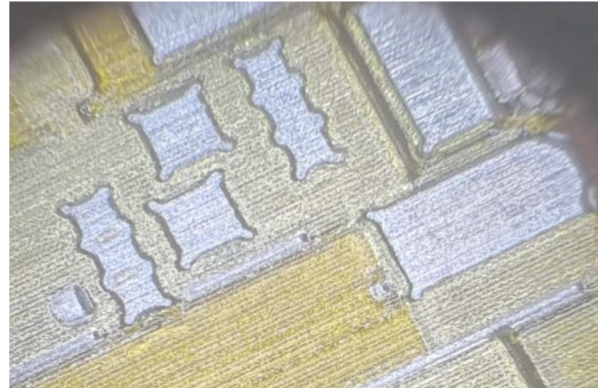


- Main 50-Ohm line



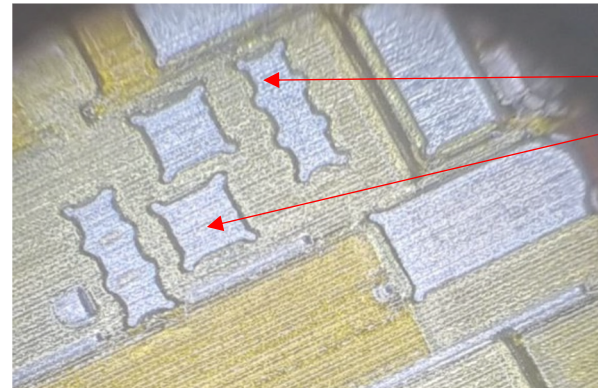
- Shielding for the RF line (walls)

Layout and BOM –cont'



- Before components placement

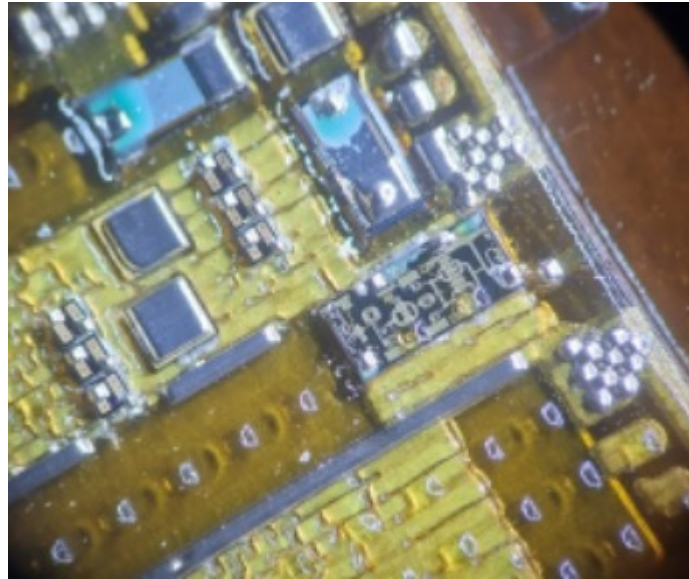
Layout and BOM –cont’



Cavities

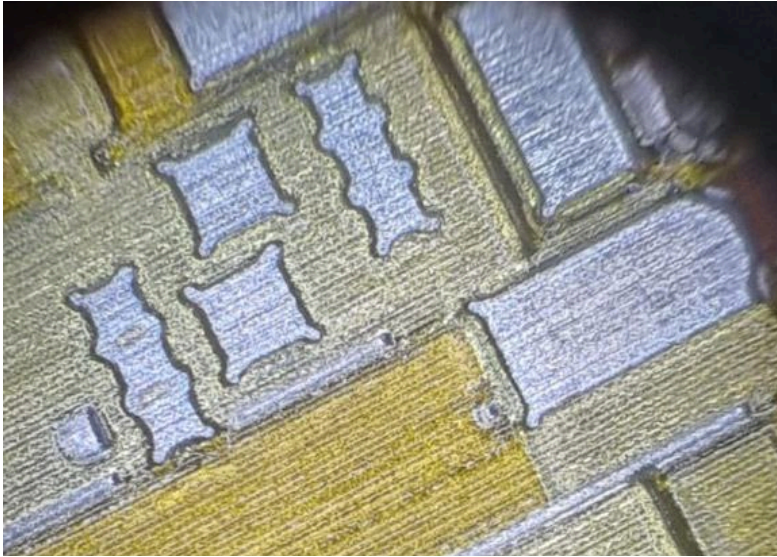
- Before components placement

Layout and BOM –cont’

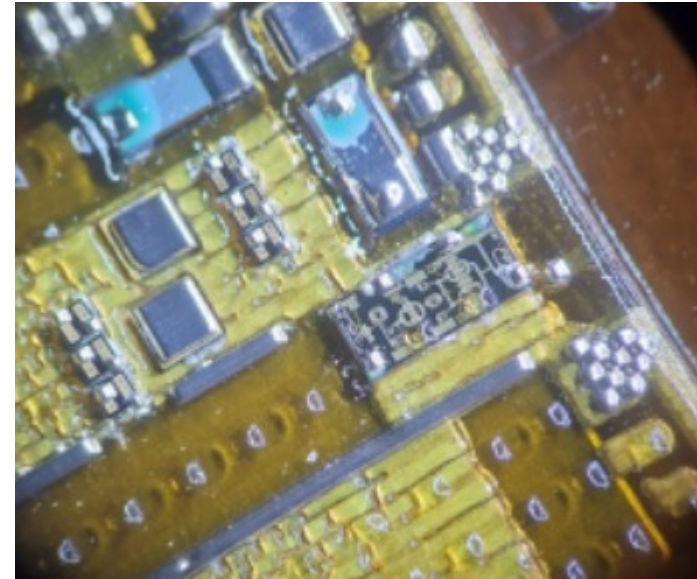


- After components placement

Layout and BOM –cont'



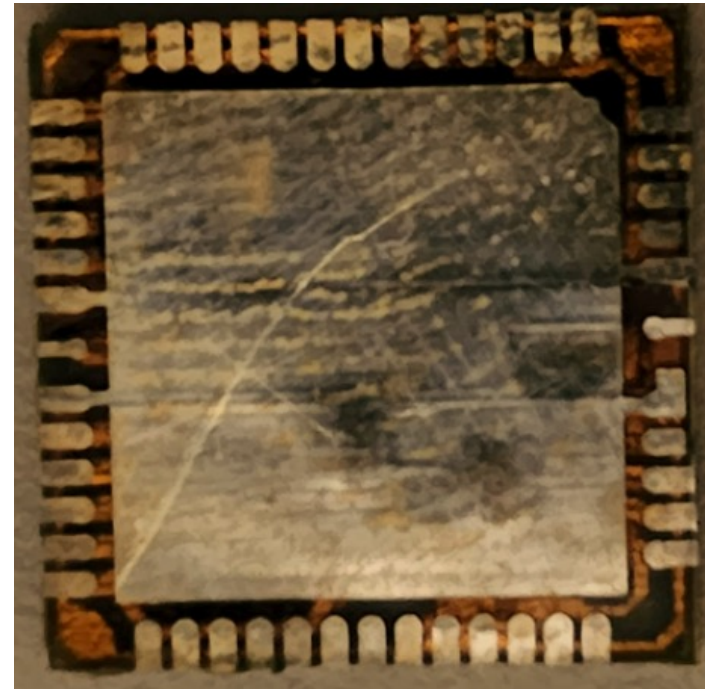
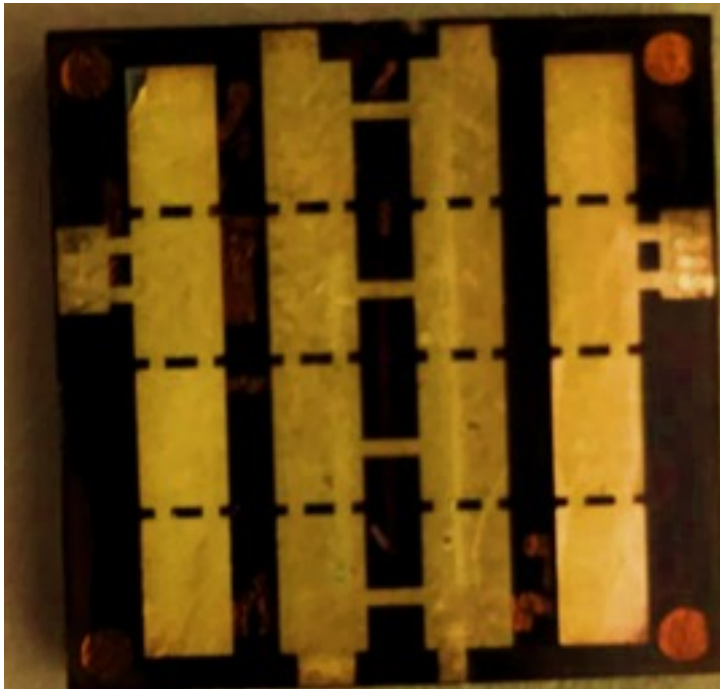
- Before components placement



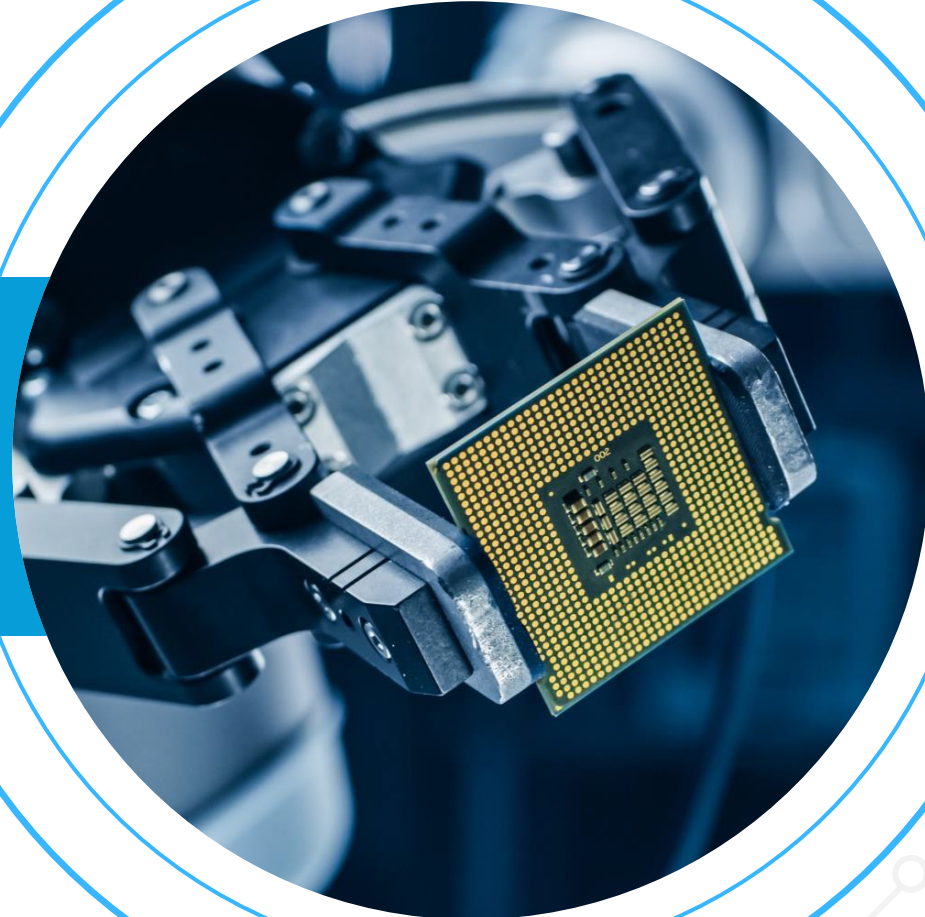
- After components placement.

Layout and BOM –cont’

- FINAL TOP & BOTTOM VIEW

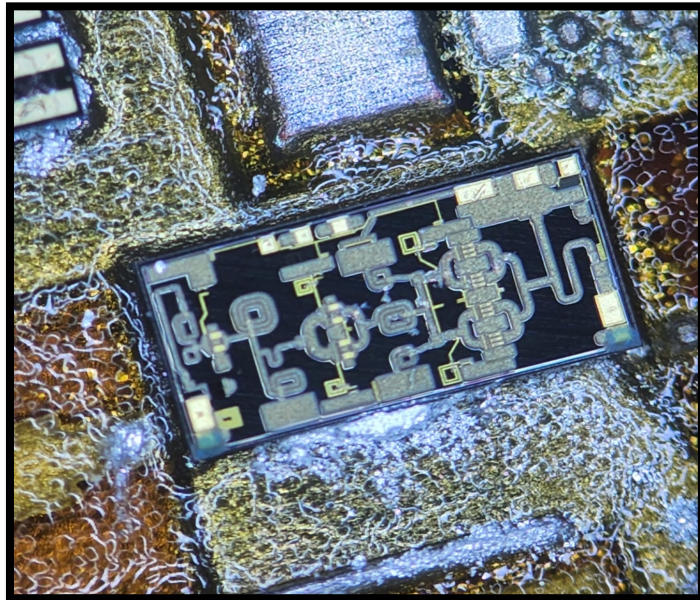


AME Packaging Processes



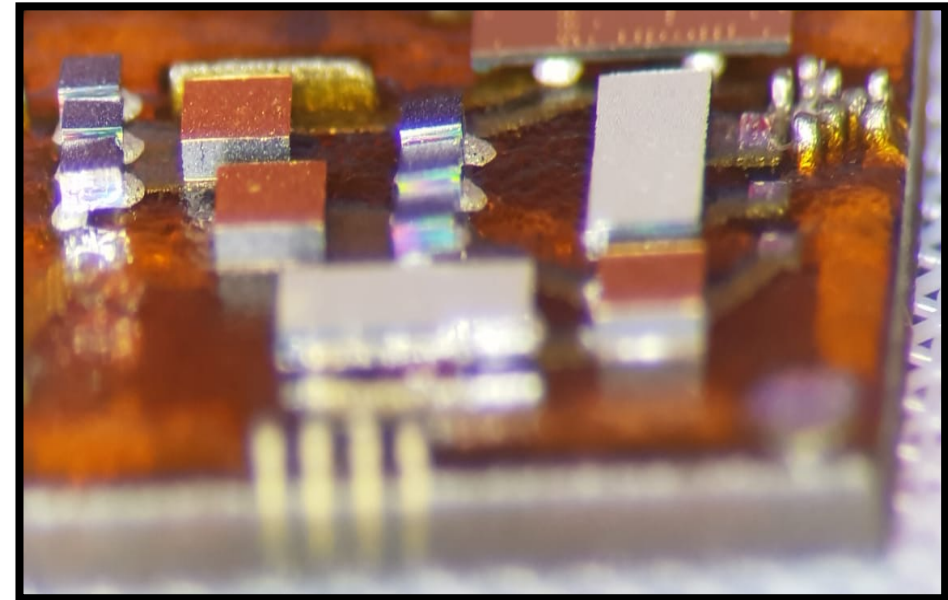
Top level processes available

Split Assembly



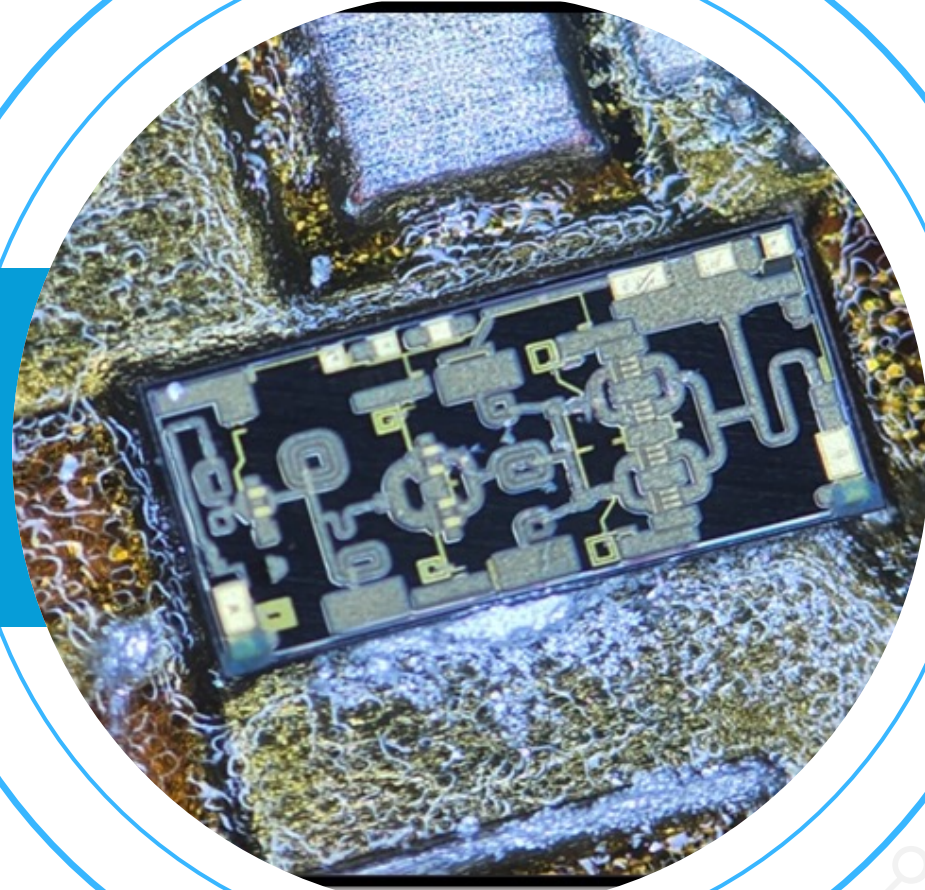
Manual placement of Die is possible

Flip Chip

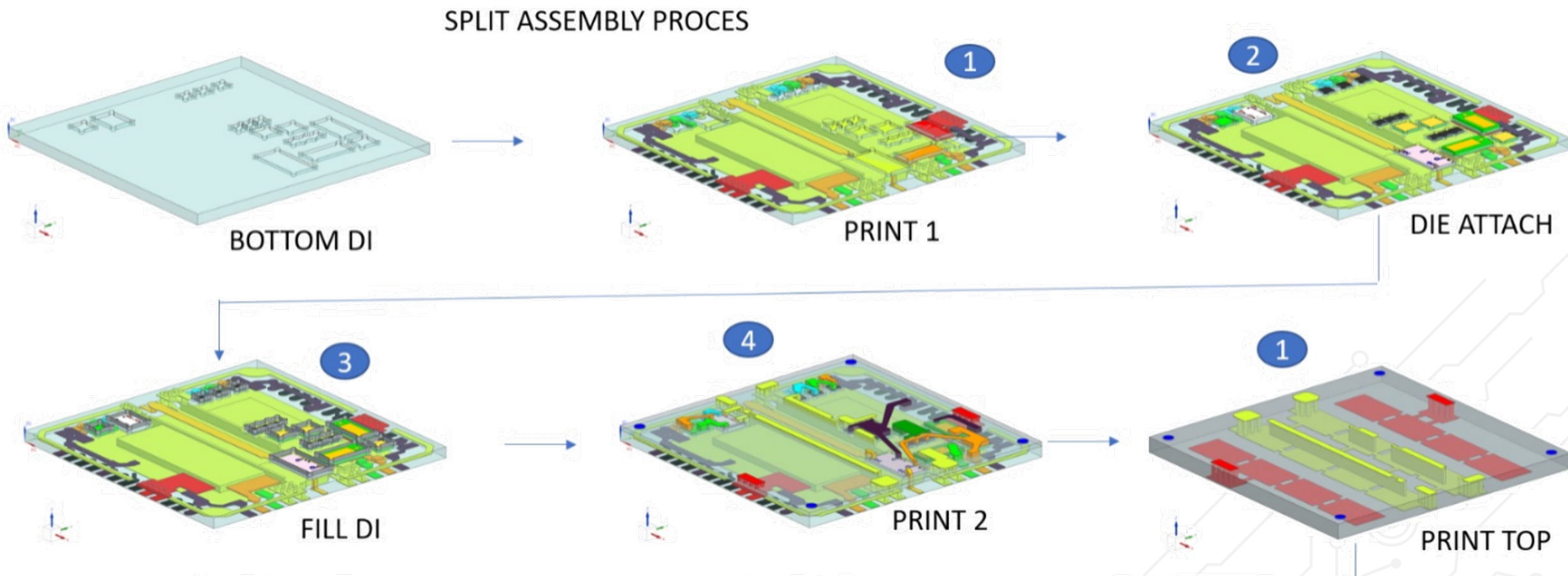


High Accuracy Automatic placement is required

Split Assembly



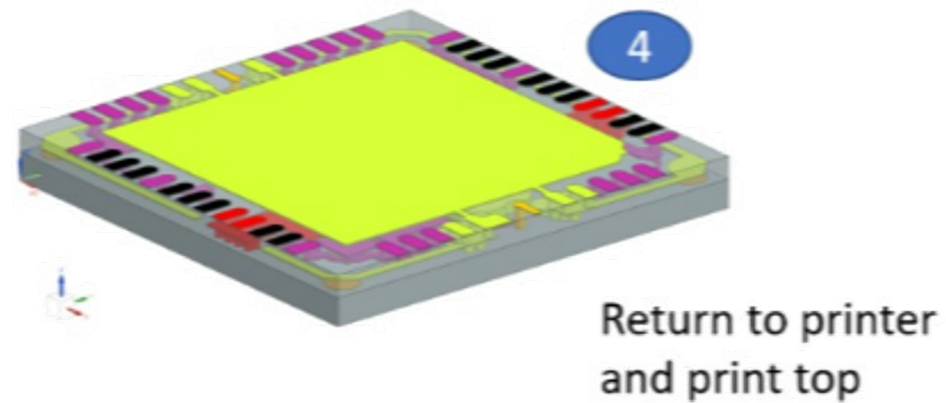
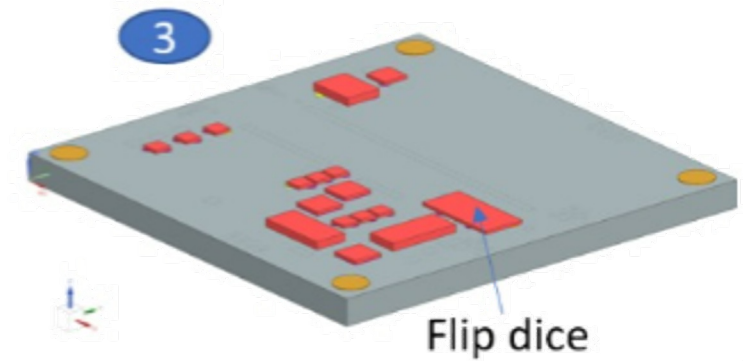
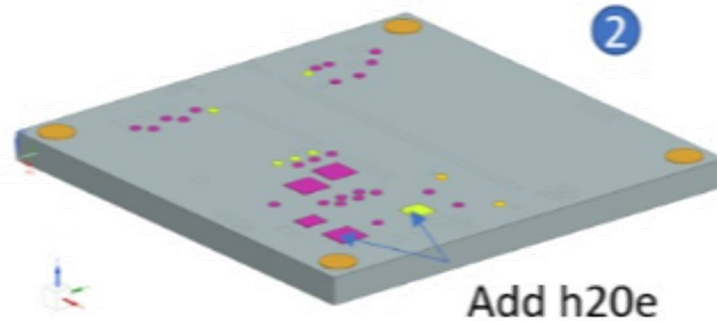
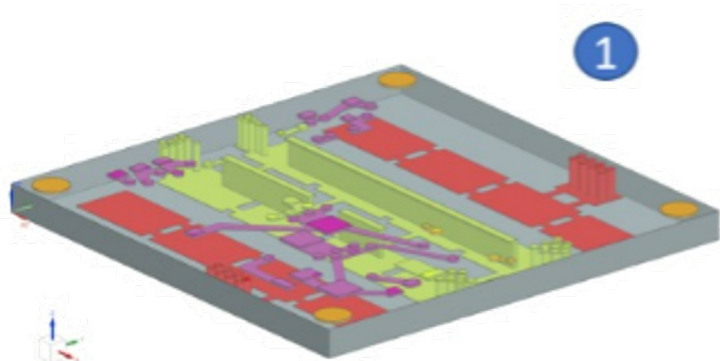
Split assembly process



Flip-Chip

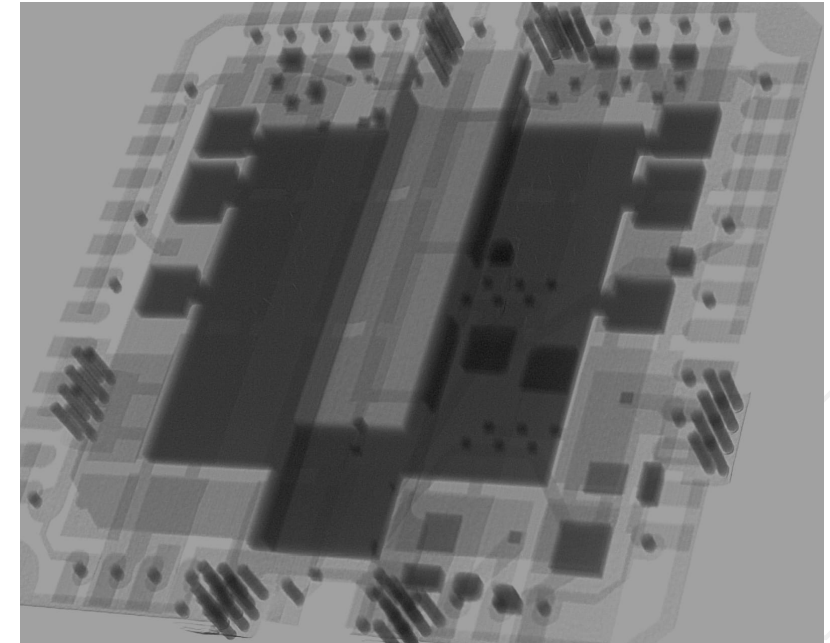
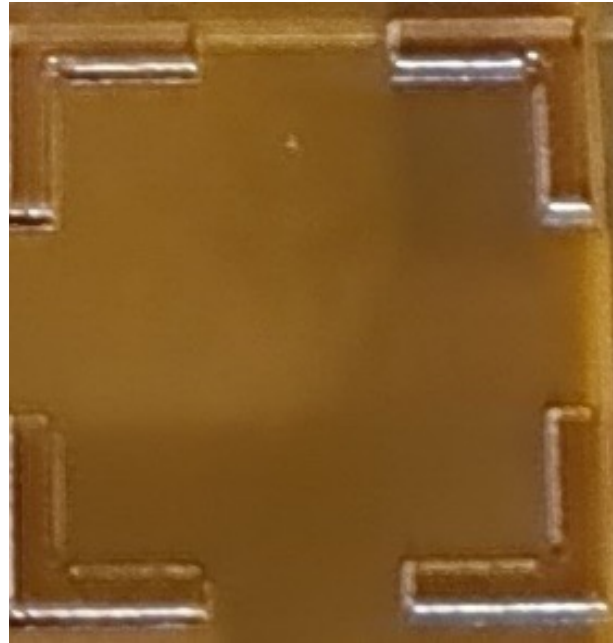


Flip chip assembly process

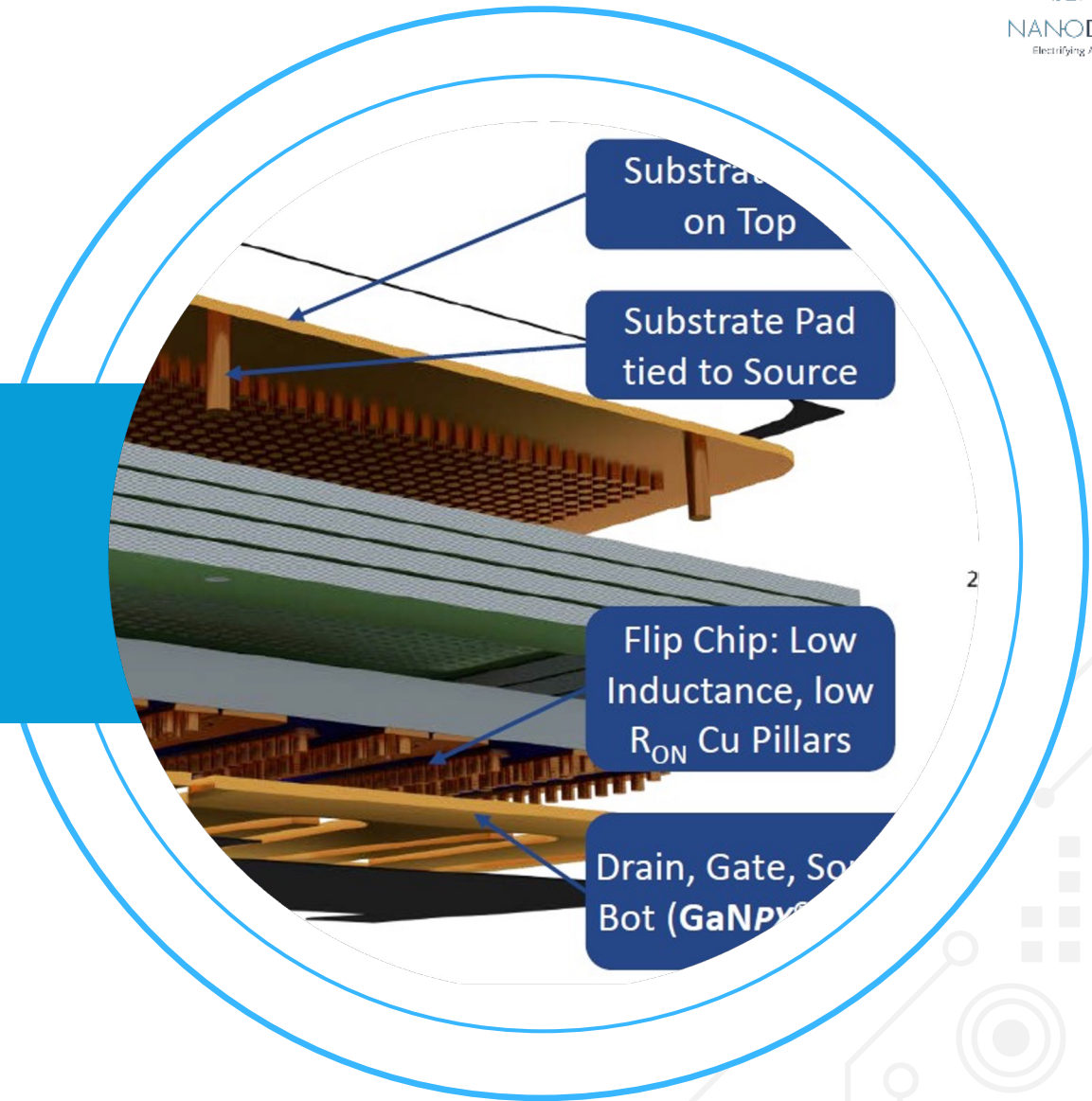


Main Process Challenges

- Registration:
 - Dies placement.
 - Building up the VIAS on top of the dies
 - Removing print for P&P.
- Pushing the current boundaries of design rules and process.



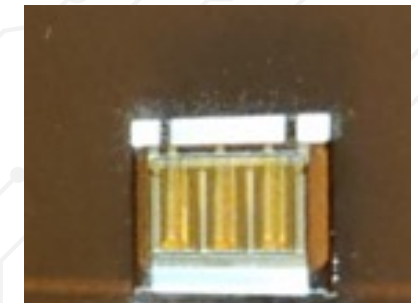
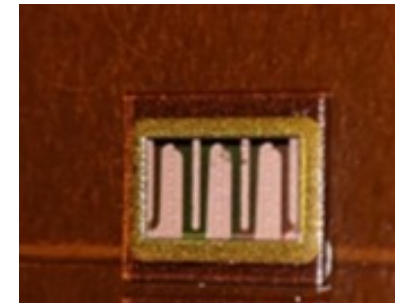
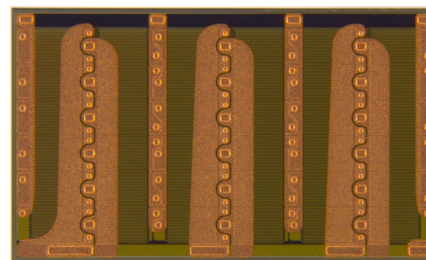
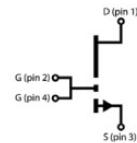
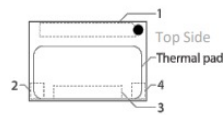
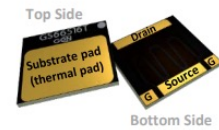
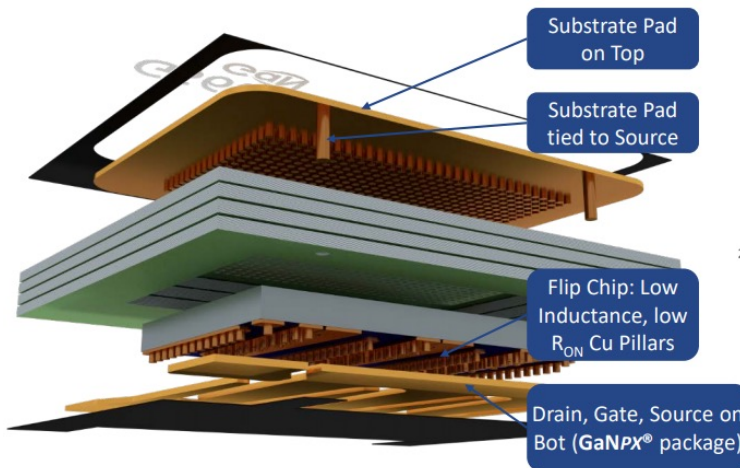
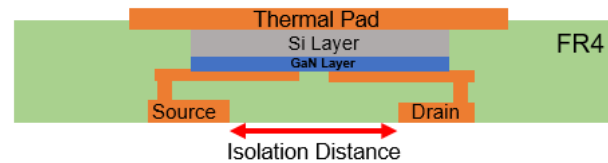
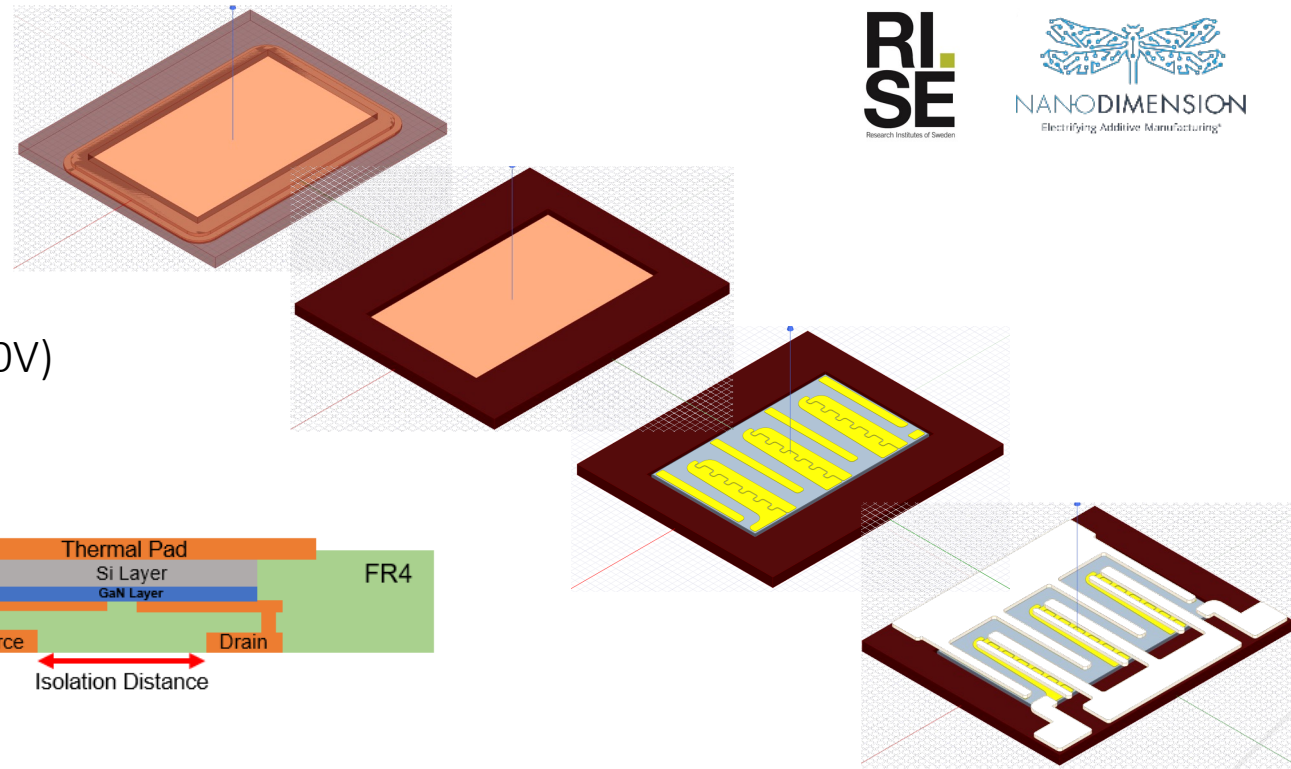
Power Transistor AME Packaging



Power Transistor SiP

GAN-ON-SILICON

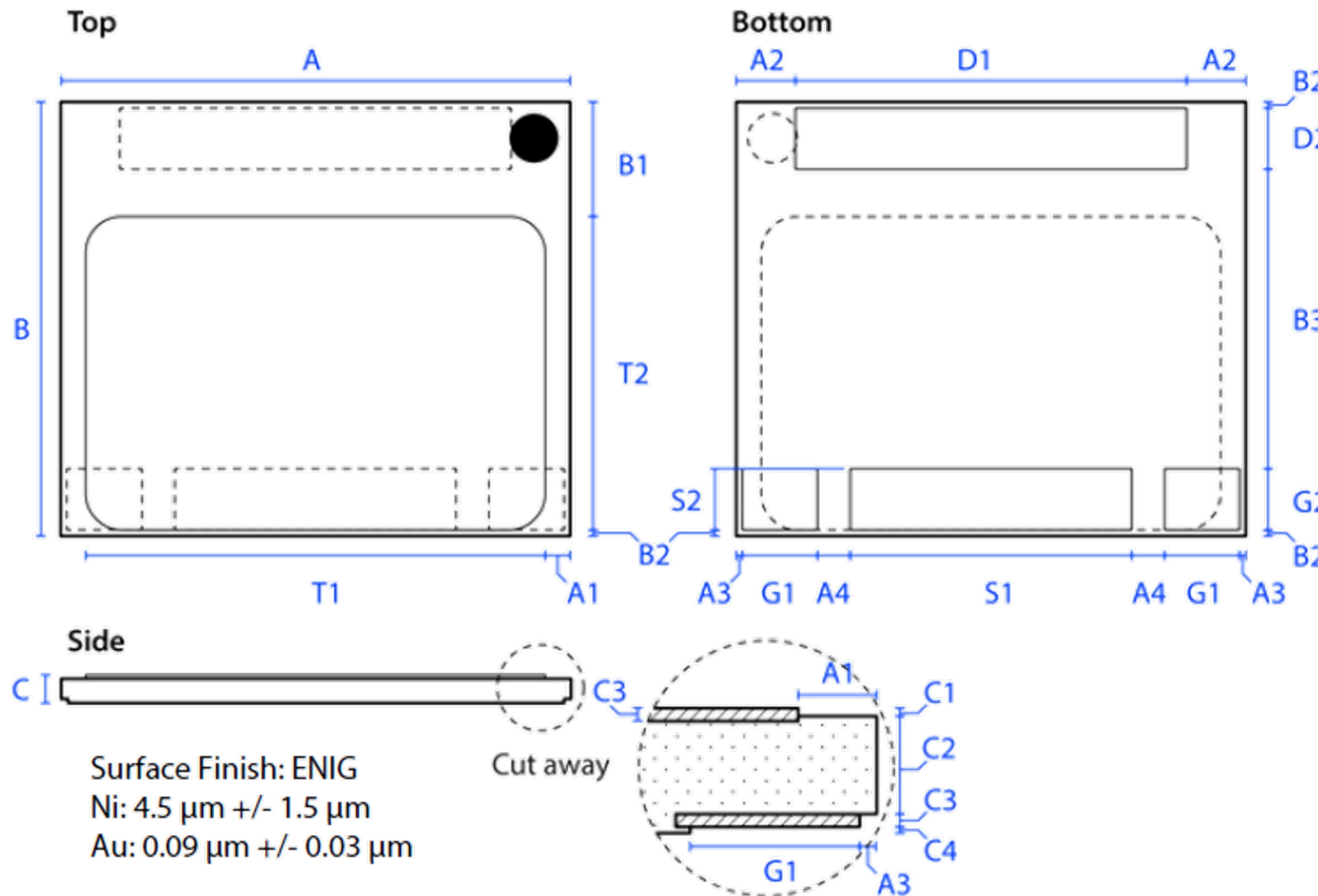
- Enhancement mode GaN-on-silicon power transistor (650V)
- Top-side cooled configuration
- High current $I_{ds(max)} = 60A$
- $R_{ds(on)} = 25m\Omega$
- Very high switching frequency ($> 100MHz$)
- Small 9 X 7.6 mm PCB footprint



Power Transistor SiP

GAN SYSTEMS (GS66516T)

Package Dimensions



	mm	Inches	
A	9.00	0.354	± 0.10 mm (0.004")
A1	0.365	0.014	± 0.05 mm (0.002")
A2	1.03	0.041	± 0.05 mm (0.002")
A3	0.075	0.003	± 0.05 mm (0.002")
A4	0.59	0.023	
B	7.64	0.301	± 0.10 mm (0.004")
B1	1.925	0.076	± 0.05 mm (0.002")
B2	0.075	0.003	± 0.05 mm (0.002")
B3	5.39	0.212	
C	0.54	0.0213	± 0.05 mm (0.002")
C1	0.04	0.0016	
C2	0.40	0.0157	
C3	0.07	0.0028	
C4	0.03	0.0012	
D1	6.94	0.273	
D2	1.05	0.041	
G1	1.30	0.051	
G2	1.05	0.041	
S1	5.07	0.200	
S2	1.05	0.041	
T1	8.27	0.326	
T2	5.64	0.222	

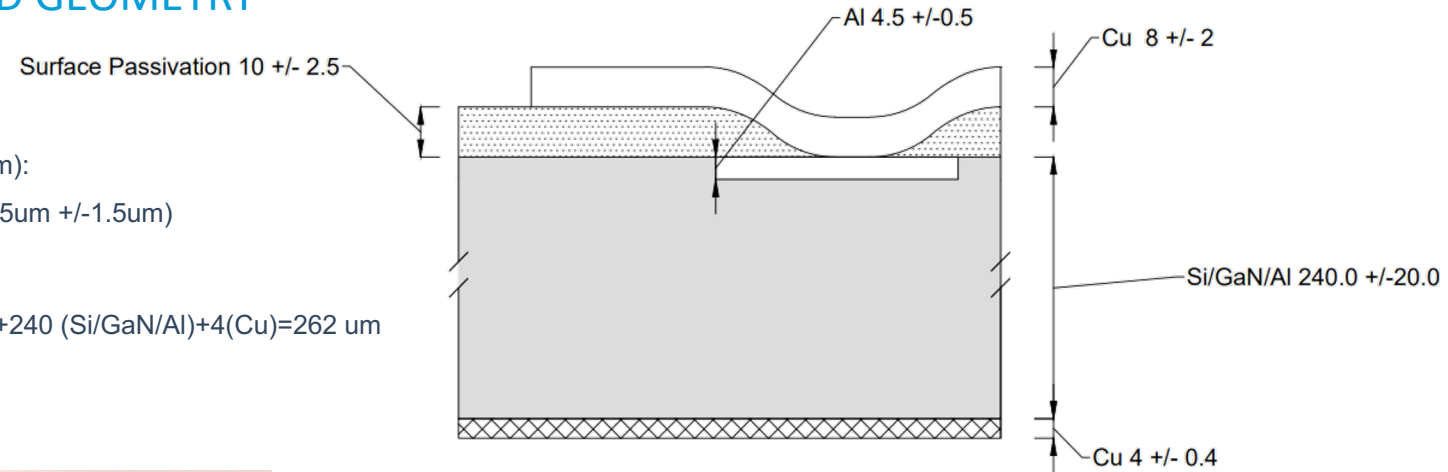
Isolation Distance

Power Transistor SiP

GAN SYSTEMS (GS66516T) PAD GEOMETRY

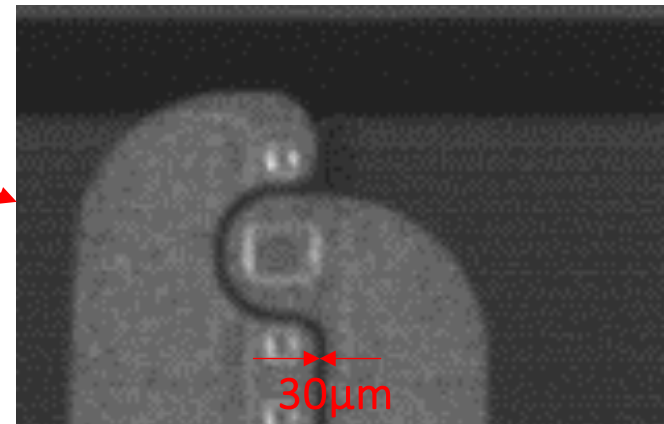
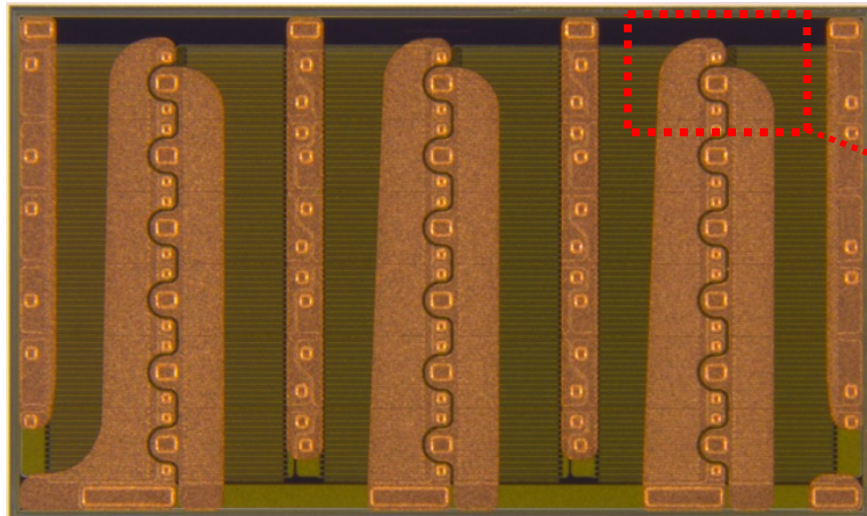
- Metallization: Cu (thickness= 8um +/- 2um)
Passivation (total thickness= 10um +/- 2.5um):
Very top passivation: polyimide (thickness= 5um +/-1.5um)
Below Polyimide: SiO₂ and SiN passivation.
- Die total thickness: 8 (Cu)+10 (Passivation)+240 (Si/GaN/Al)+4(Cu)=262 um

X-X Cross section



Units = μm

- Topside Metallization
- Passivation
- Exposed Si Substrate
- Backside Metallization

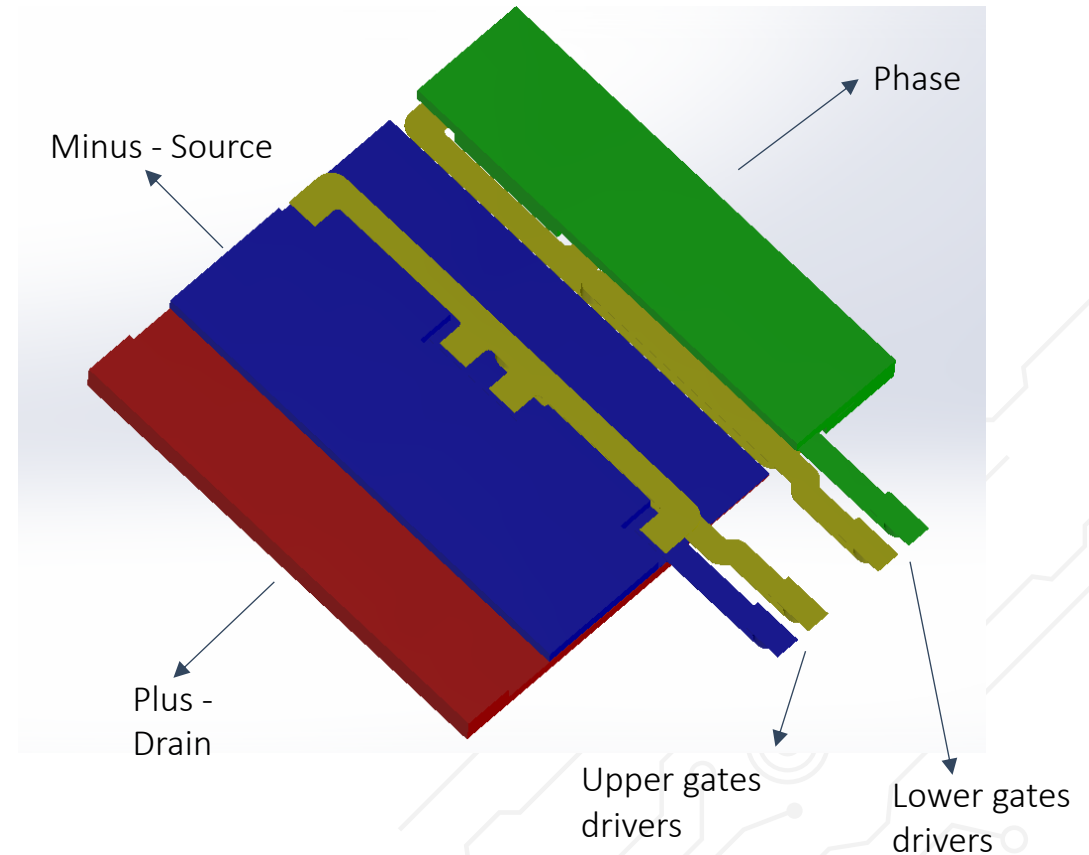
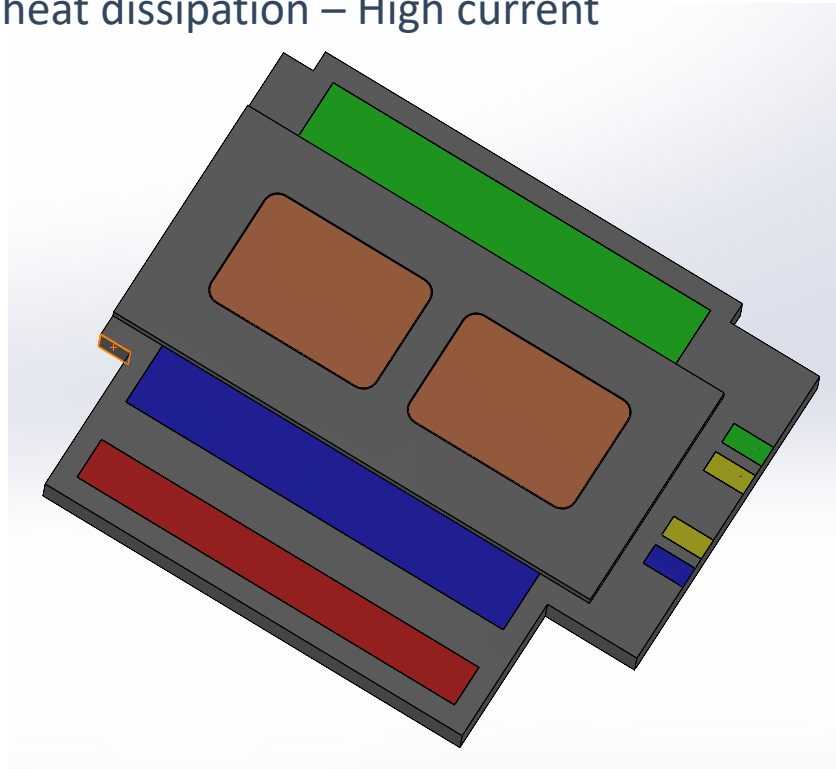


Power Transistor SiP

RI.SE DESIGN FOR AME

Challenges:

- Meeting the application targets – High voltage, high current
- Effective heat dissipation – High current

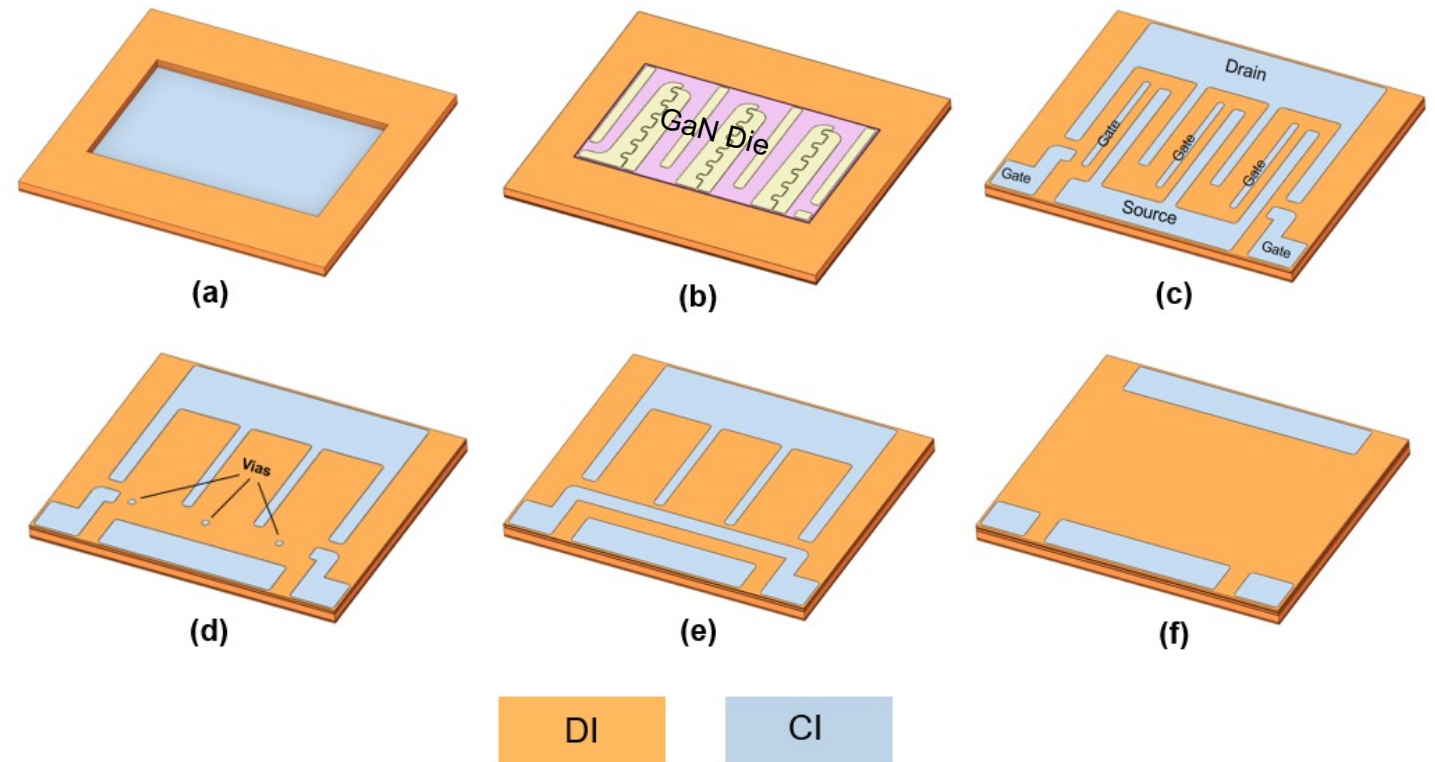


Power Transistor SiP

GAN-ON-SILICON

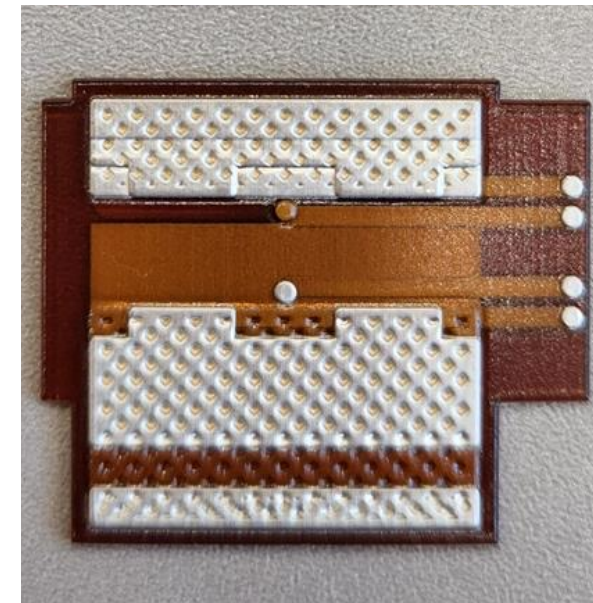
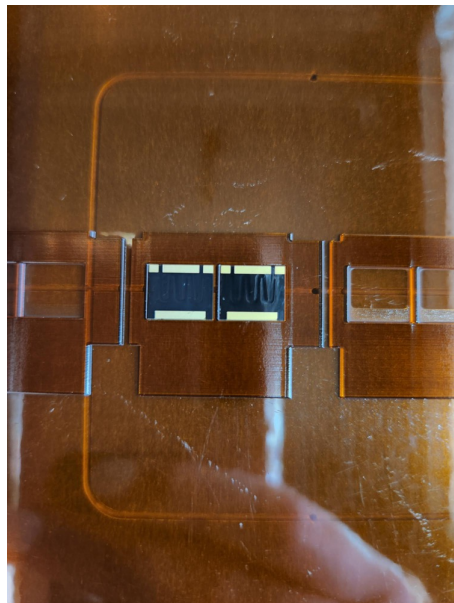
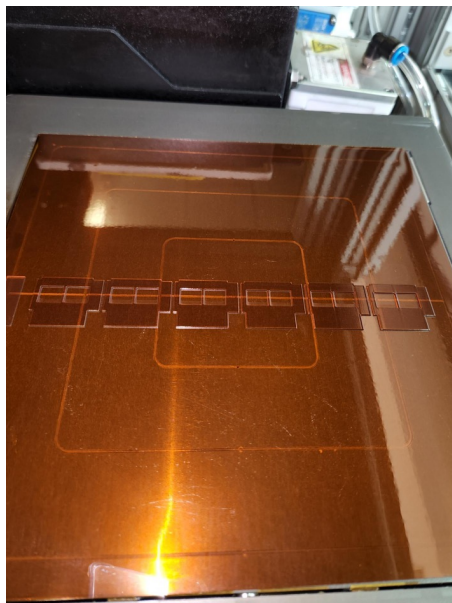
Process:

- Printing dielectric cavities & pause the print (keeping chuck at 100°C)
- Placing the silicon dies and adding Epotek conductive glue on the bare pads
- Print DI “soldermask alike” and fill gaps
- Print CI pads connection
- Print interconnecting tracks
- Print cover layer



Power Transistor SiP

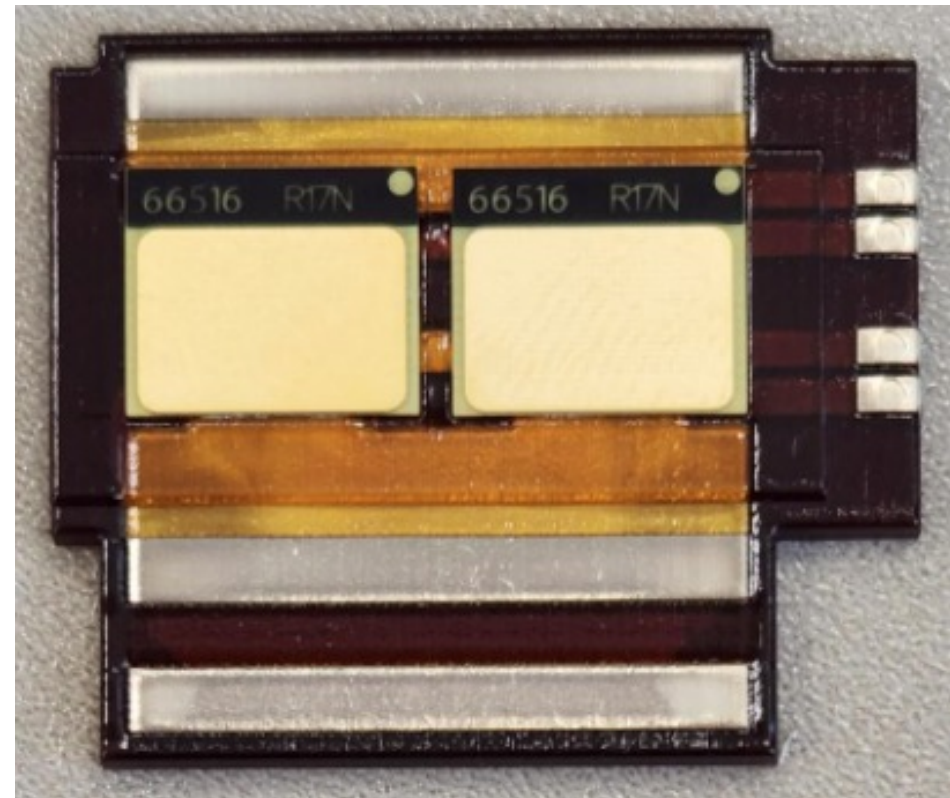
GAN-ON-SILICON



Power Transistor SiP

GAN-ON-SILICON

Resulting package

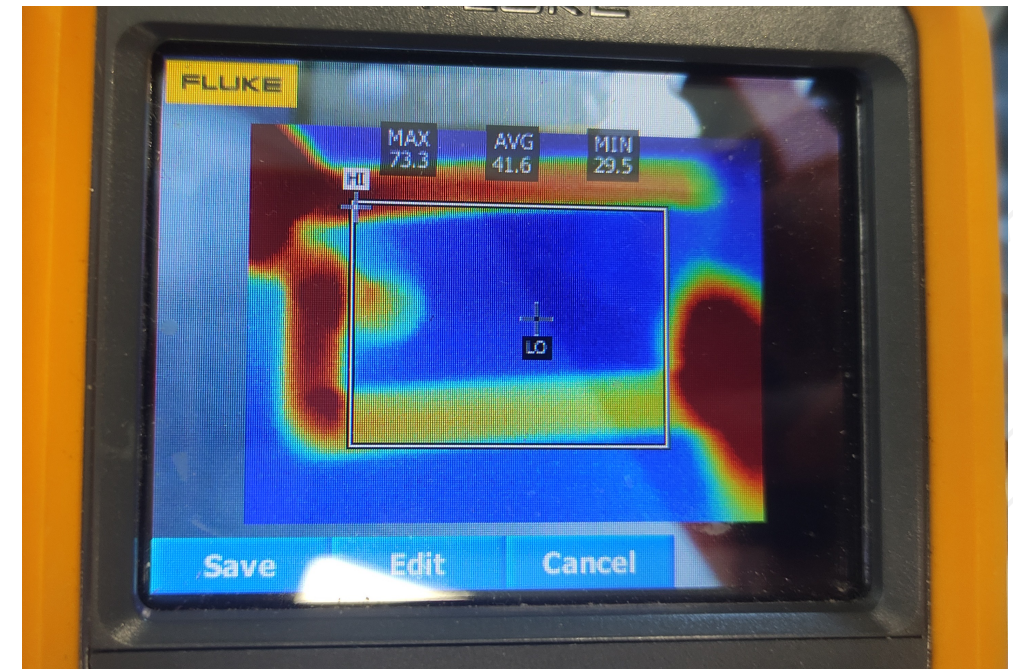
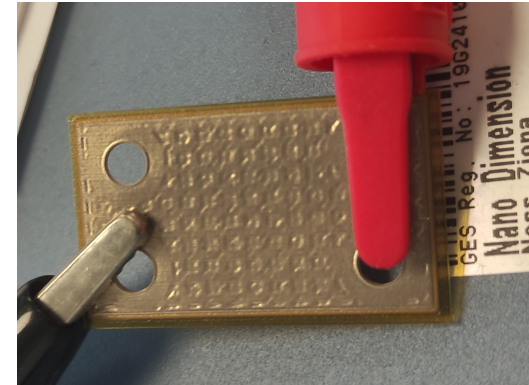


Power Transistor SiP

GAN-ON-SILICON

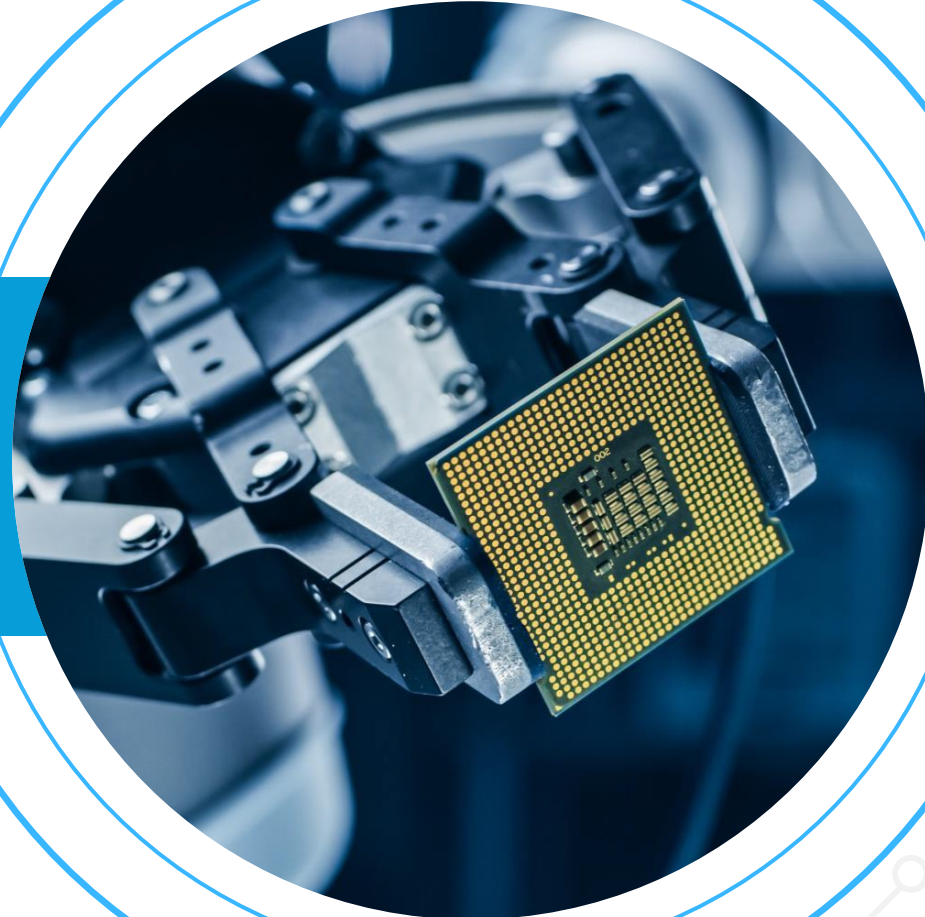
Tests:

- 38Amp @ room temp (25°C)



NFC

Summary



Nano's Footprint in Silicon Packaging

SIGNIFICANT IMPROVEMENT IN GTM TIME + SPEC

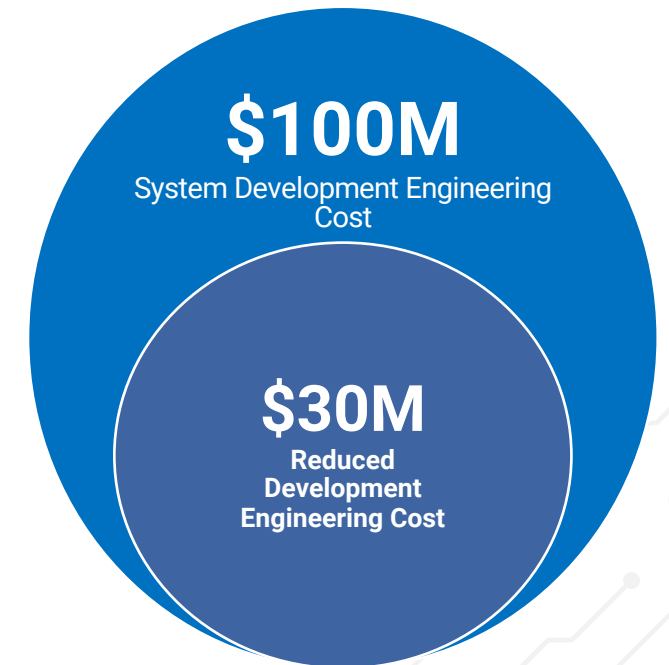
R&D cycle – 90% down



Testing cycle optimization – Test silicon device during development stage



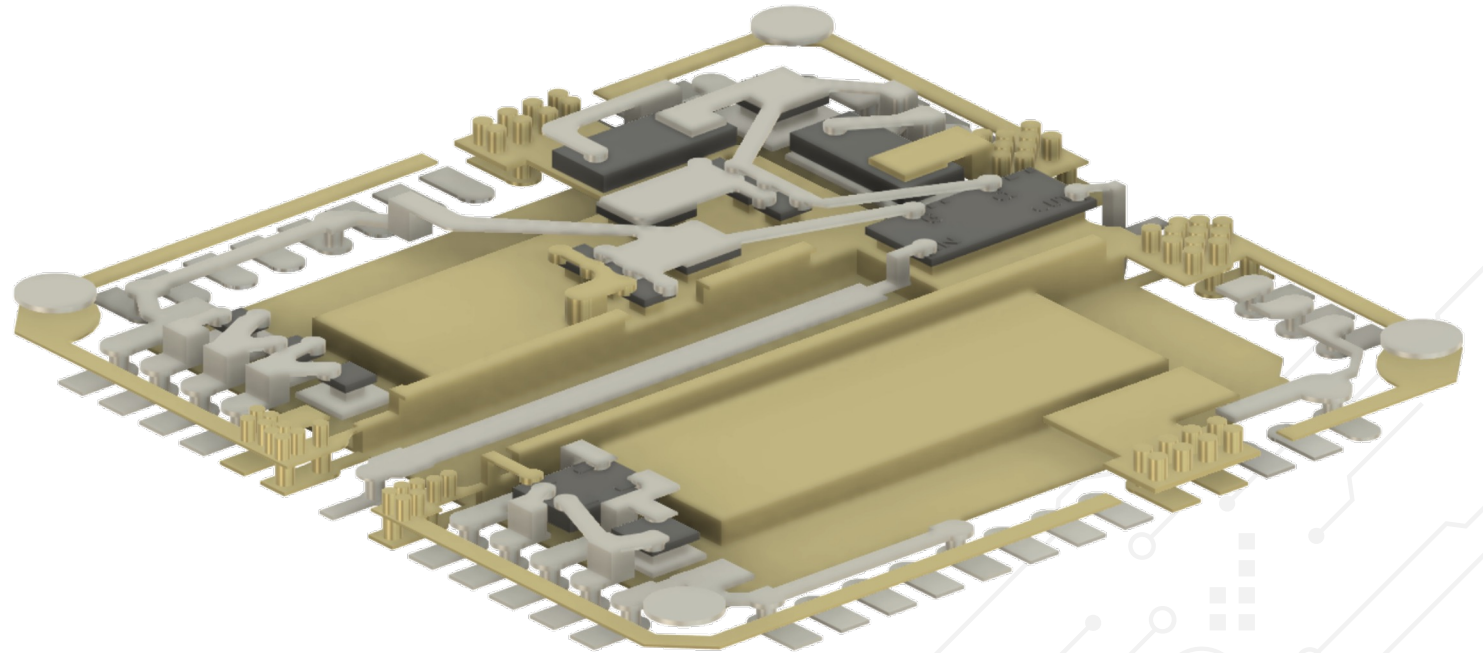
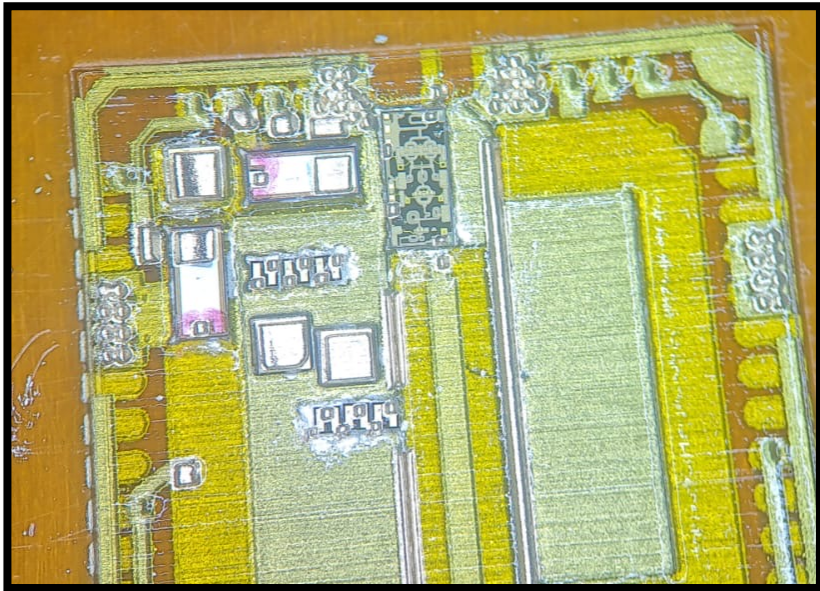
Estimated prototyping market size



Nano's Footprint in Silicon Packaging (cont.)

PERFORMANCE IMPROVEMENT

- Wirebondingless connections: Transmission lines' interconnects can be controlled by design

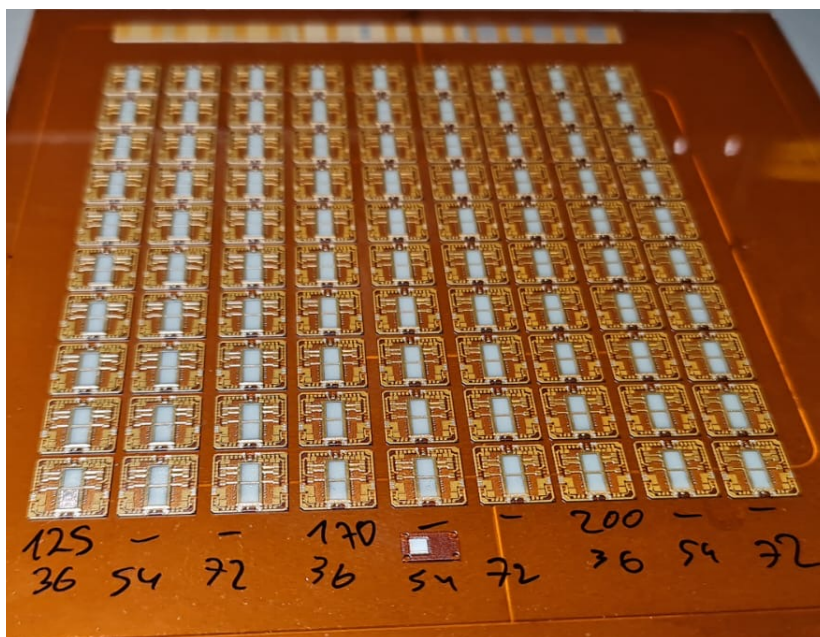


SiP & Packaging Market Share

FUTURE - PROCESS PLANNING, SYSTEM DESIGN AND DIE IMPLEMENTATION

Further improvements towards production

With improvement of our materials, We can produce immediate high mix low volume RF SiPs



SiP production market size

Growing market – 8% CAGR till 2030

\$34.2B

Largest Market: North America

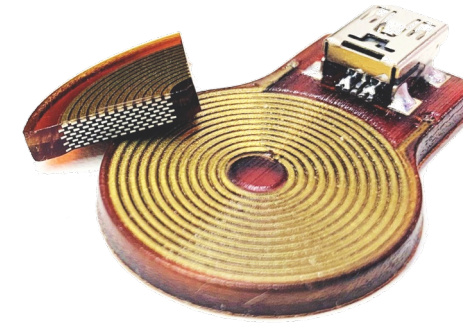


*With few big legacy players, it's a highly concentrated market, ready to be disturbed

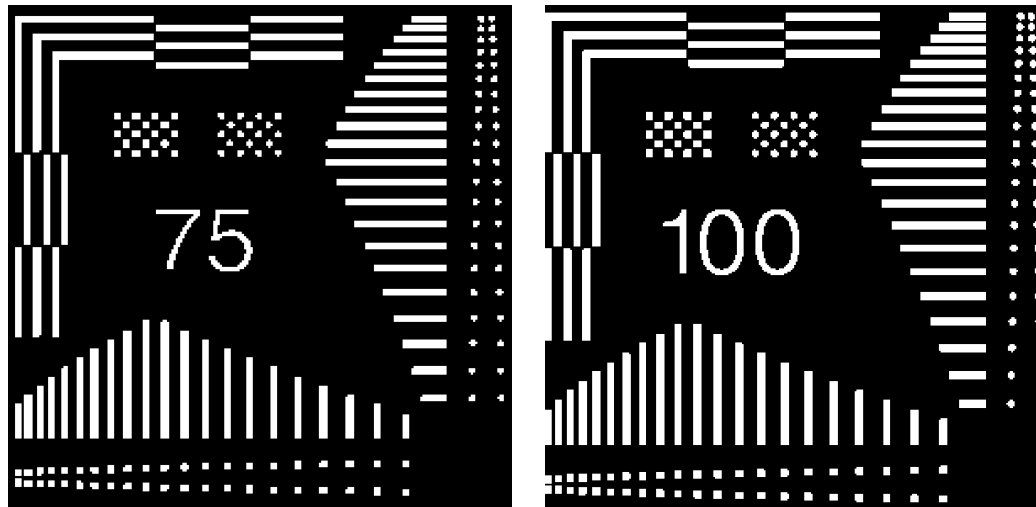
Thank you!

UNLEASH AME POTENTIAL – APPLIED PHYSICS

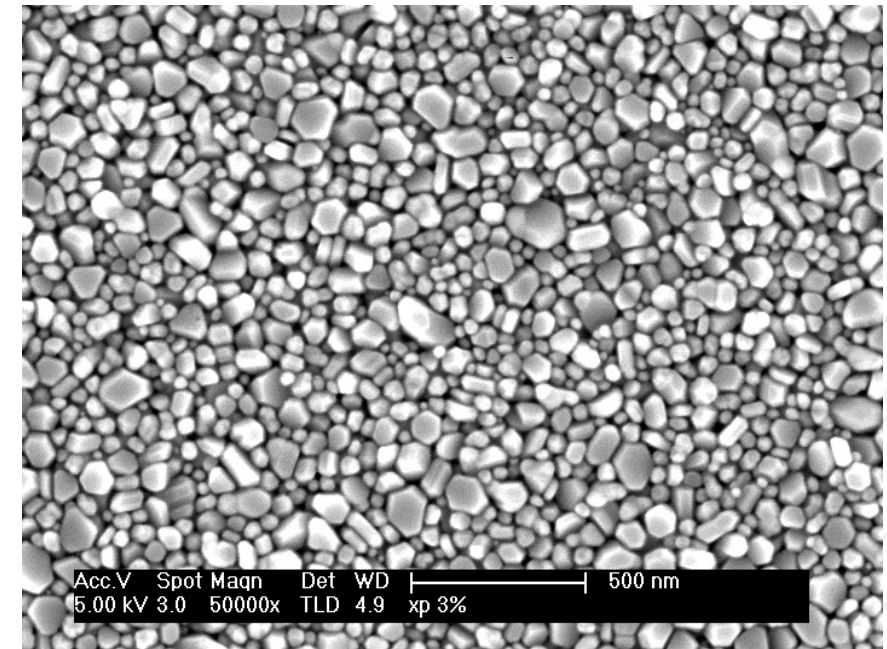
- Dimensional accuracy, slice over slice.
- AgCite™ Nanoparticle Silver Ink



DragonFly IV & FLIGHT



Resolution Accuracy coupons



Electron microscope shot of Ag Nanoparticles